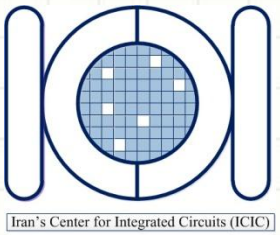
Digital Design Flow

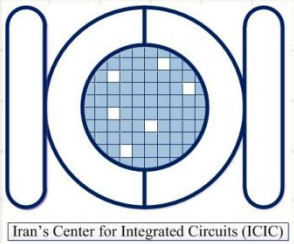
For EDA Tools:
Synopsys Design Compiler
Cadence SOC Encounter

July 2012

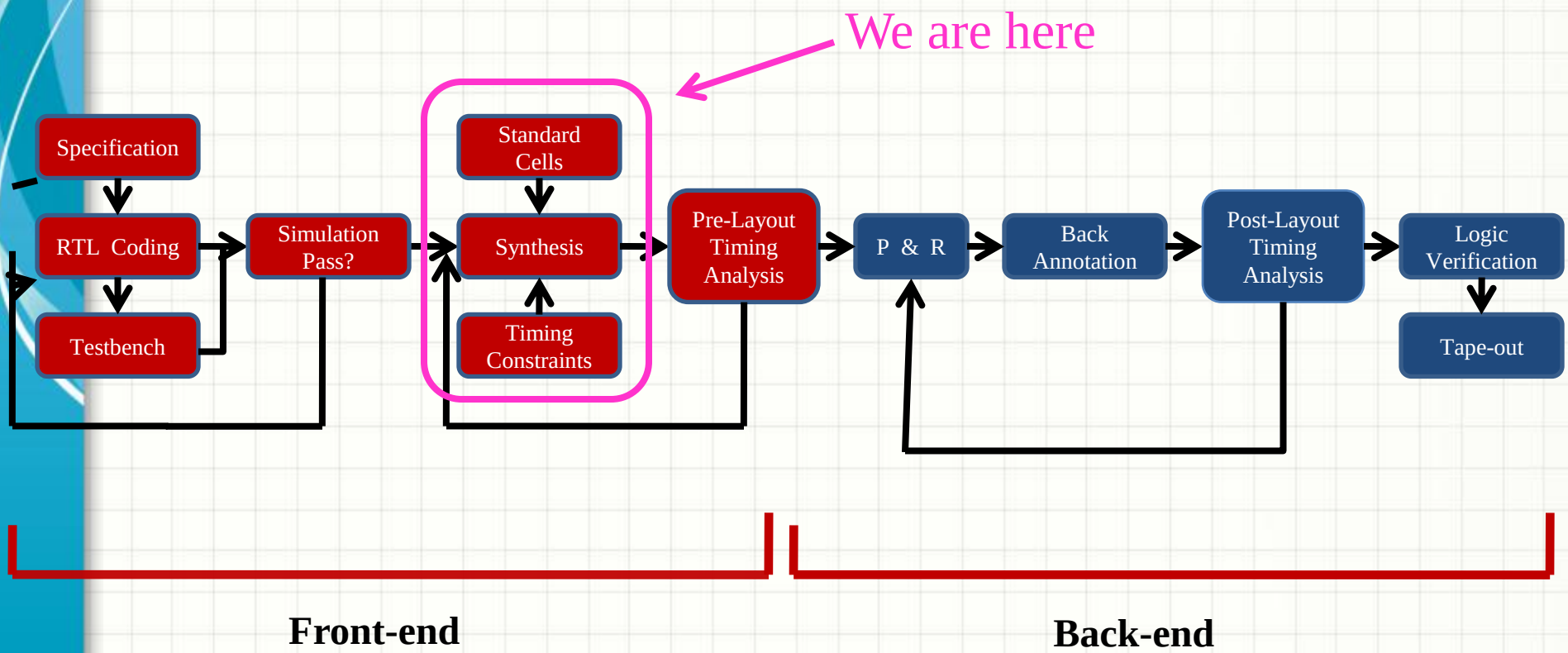


LOGIC SYNTHESIS

SYNOPSYS DESIGN VISION



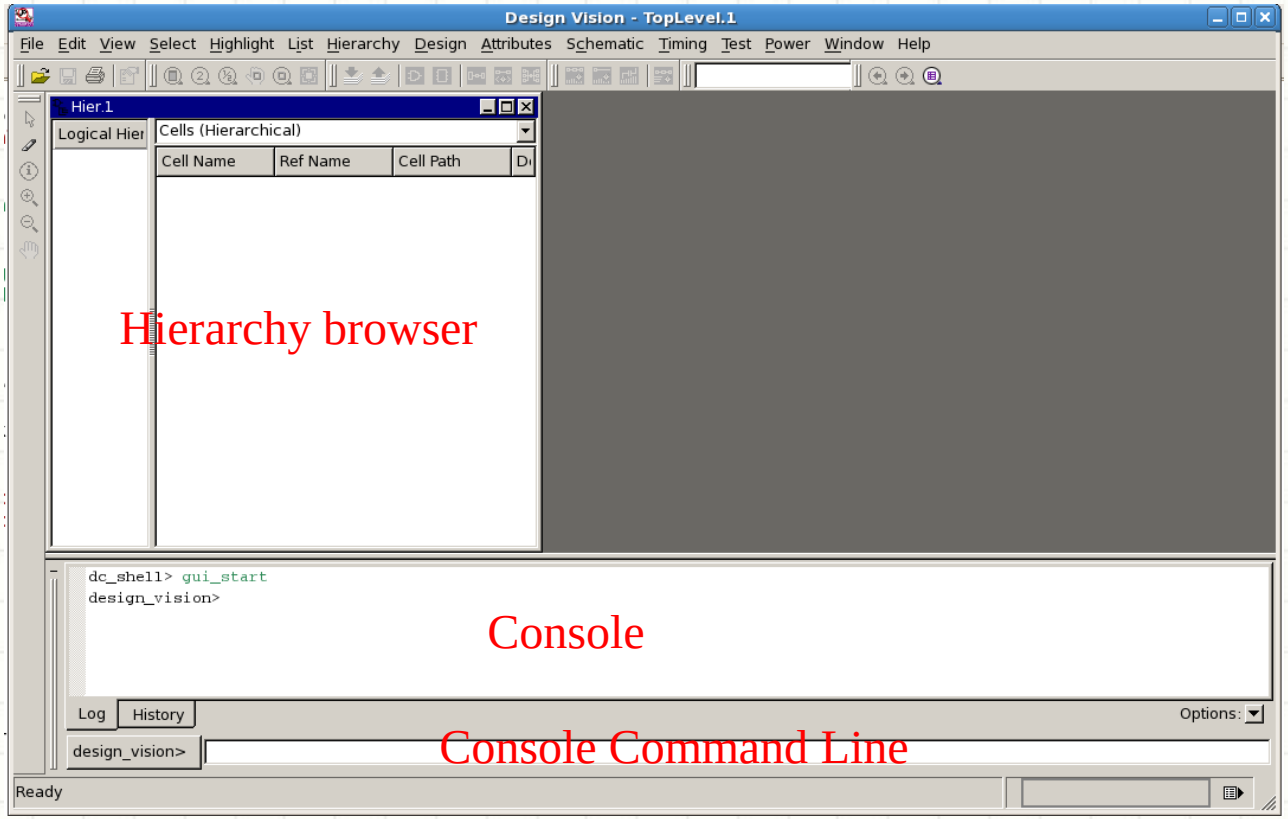
Digital Design Flow



Iran's Center for Integrated Circuits (ICIC)

Starting Design Vision

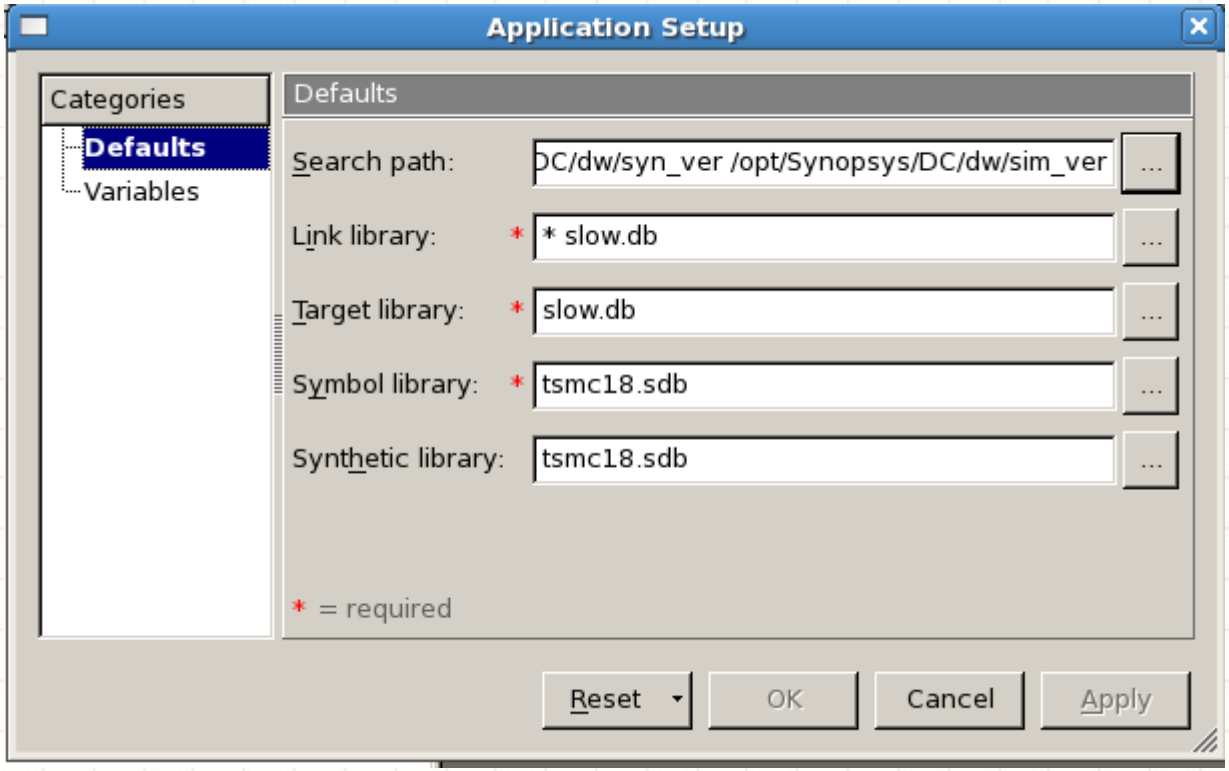
```
[user#@ICICHP home]$ cd digital_workshop/synthesis
[user#@ICICHP synthesis]$ design_vision
```



Iran's Center for Integrated Circuits (ICIC)

Setup

File -> Setup

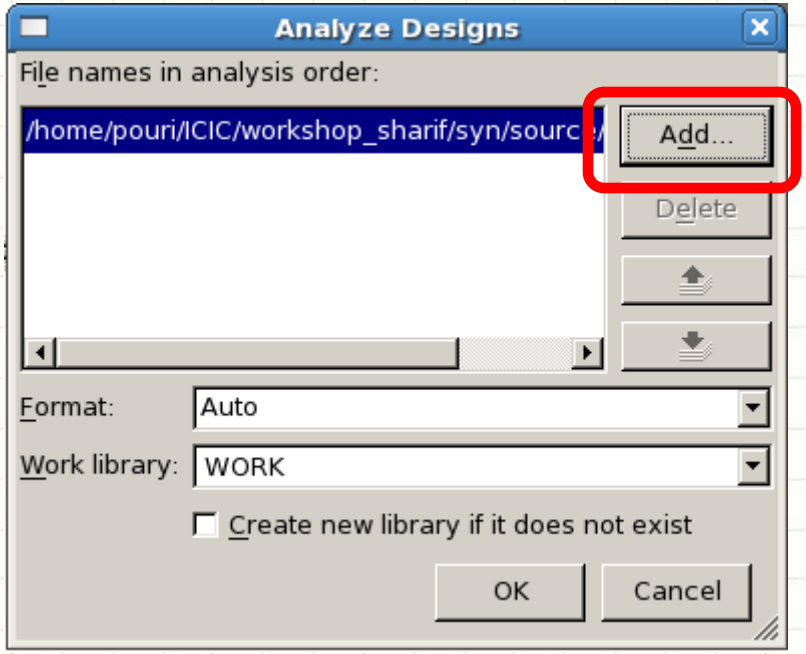


/home/pouri/digital_workshop/synthesis/.synopsys_dc.setup

Iran's Center for Integrated Circuits (ICIC)

RTL HDL Model Analysis

File -> Analyze

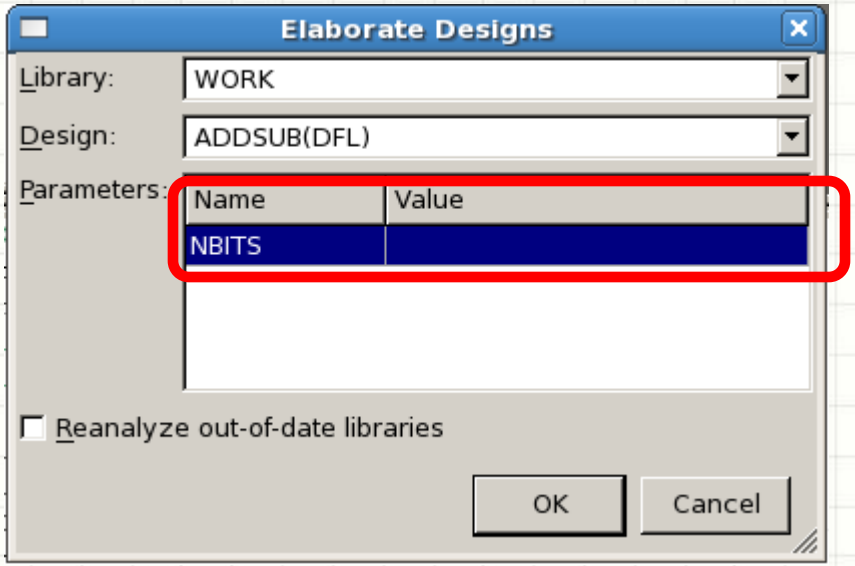



```
analyze -library WORK -format vhdl
```

Iran's Center for Integrated Circuits (ICIC)

Design elaboration

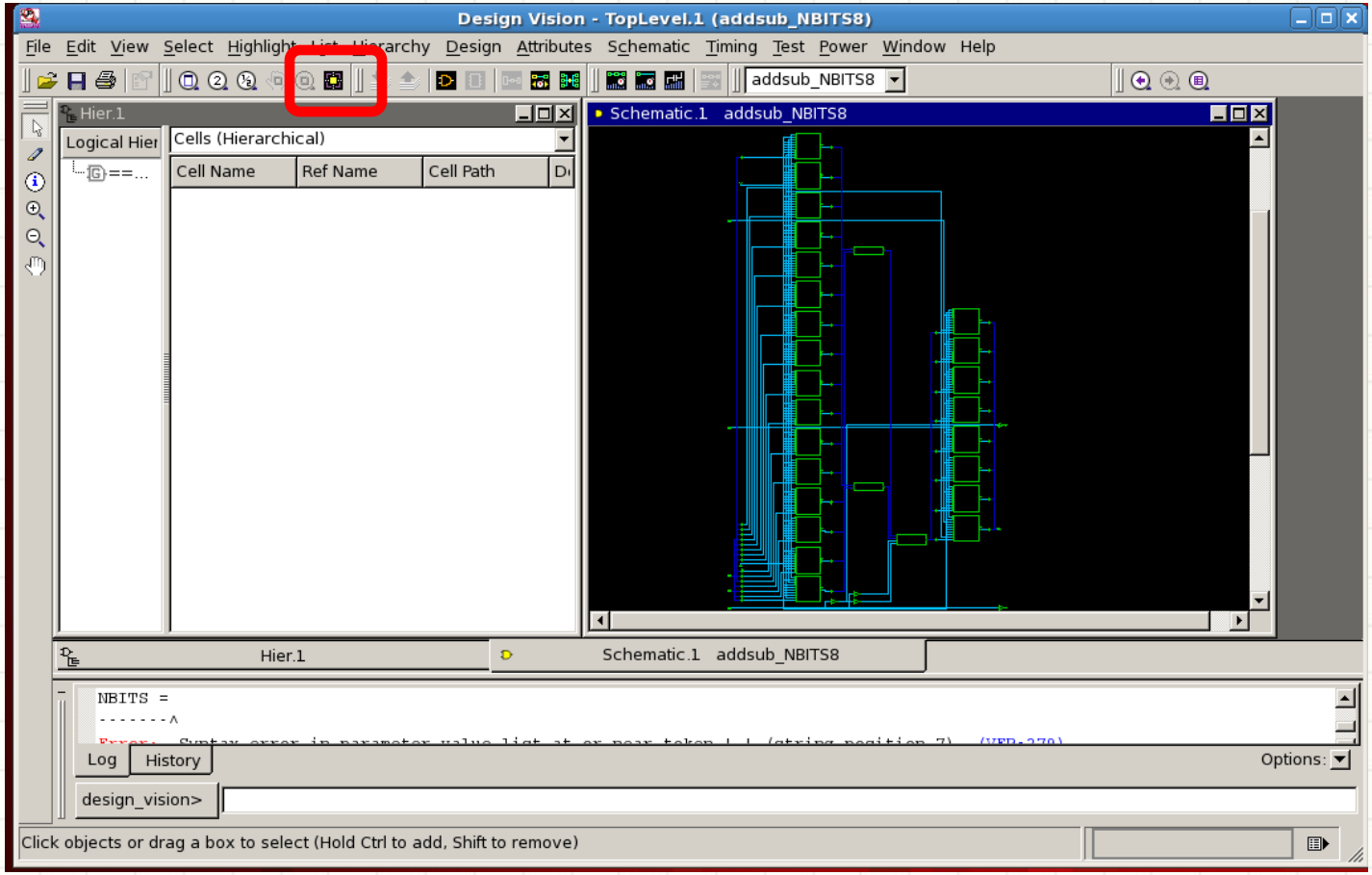
File -> Elaborate




```
elaborate ADDSUB -architecture DFL -library WORK -parameters
   "NBITS = 8"
```

Iran's Center for Integrated Circuits (ICIC)

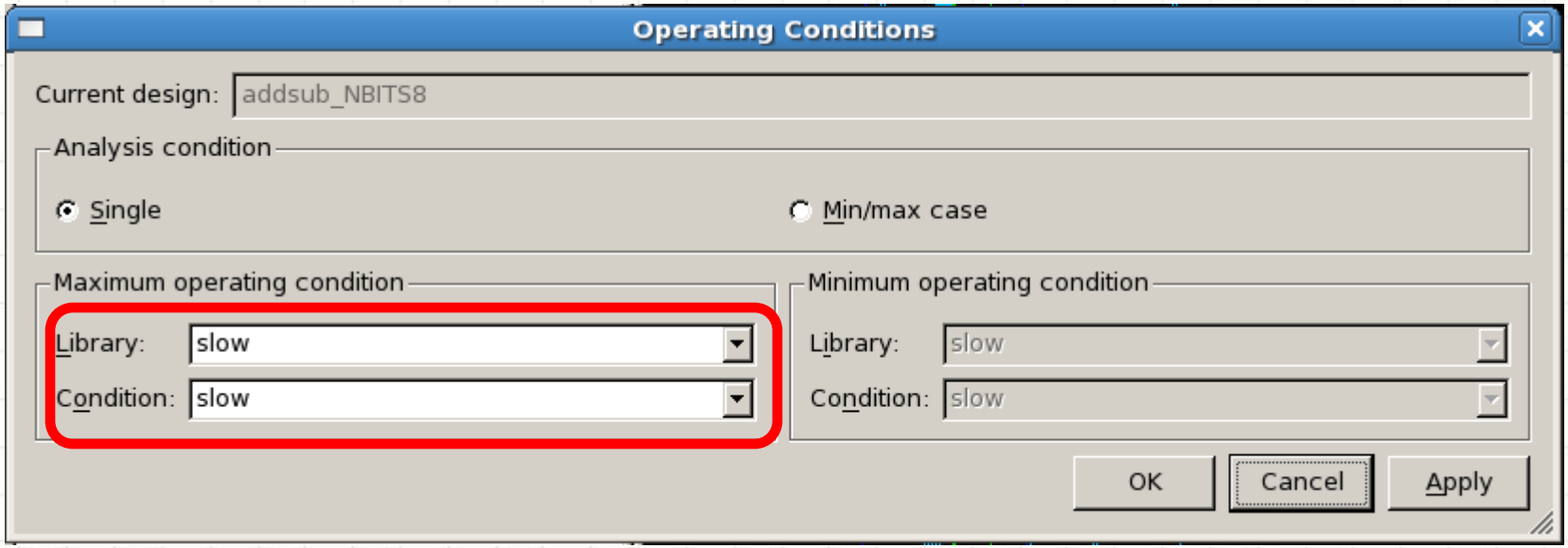
Create design Schematic



Iran's Center for Integrated Circuits (ICIC)

Design Environment Definition

Attributes -> Operating Environment -> operating Condition

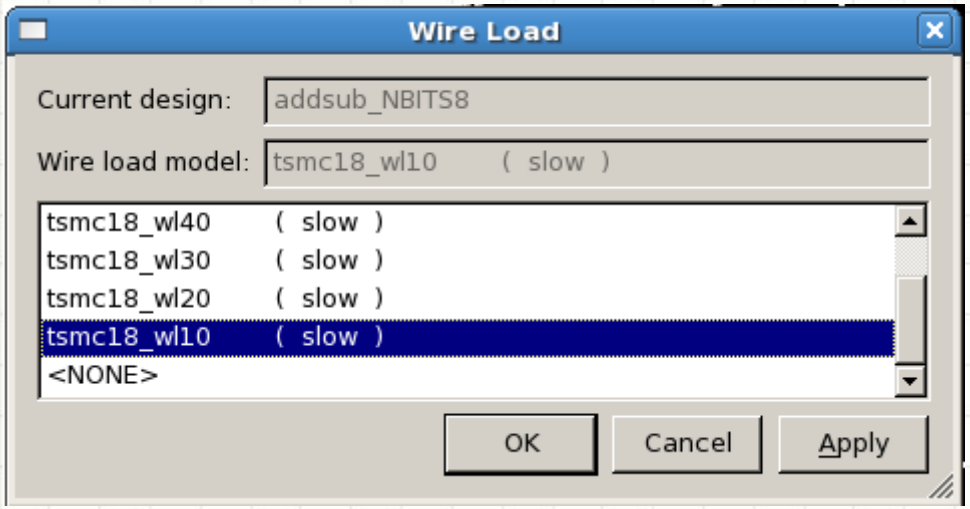



```
set_operating_conditions -library slow slow
```

Iran's Center for Integrated Circuits (ICIC)

Design Environment Definition

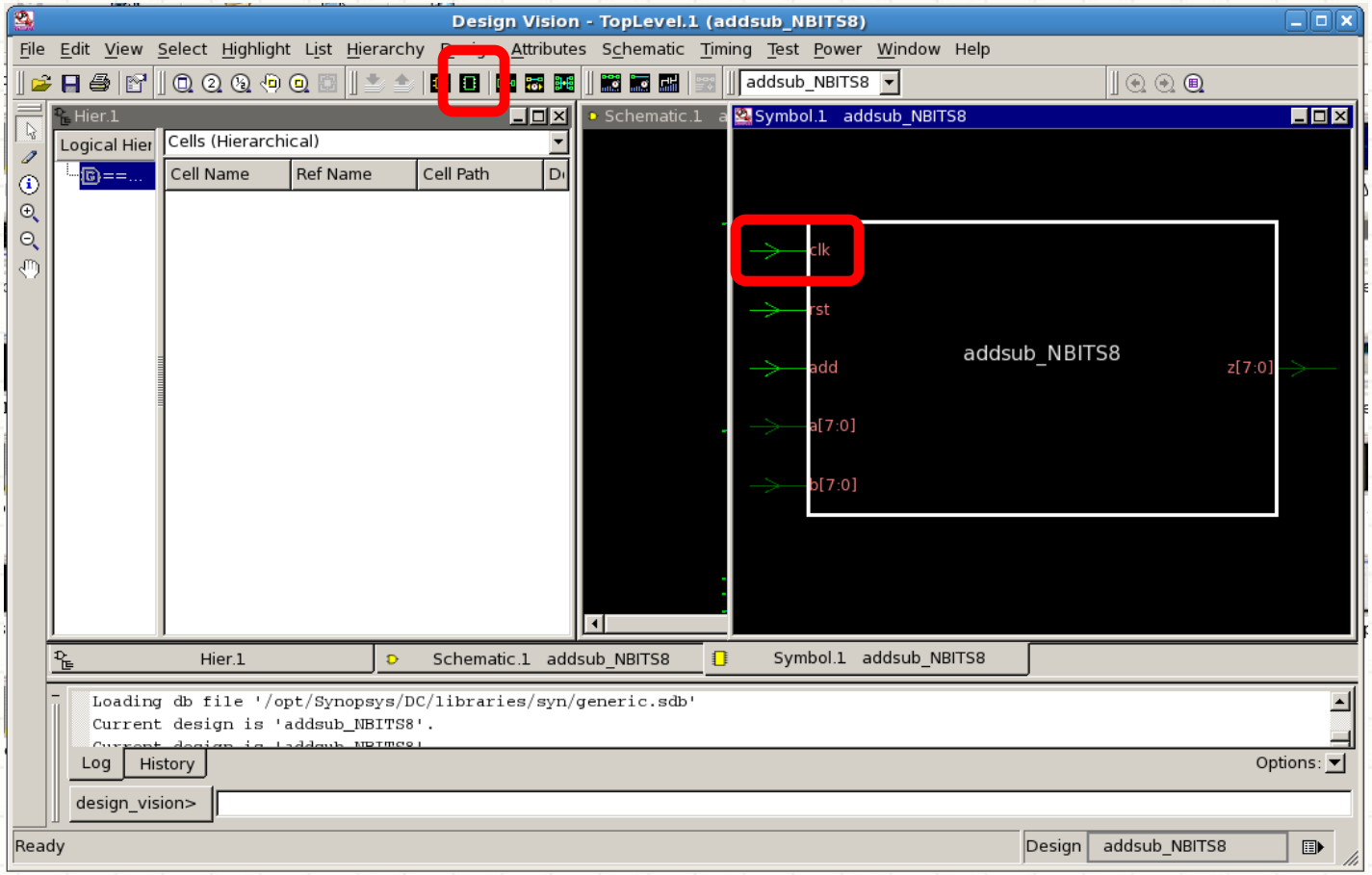
Attributes -> Operating Environment -> Wire Load




```
set_wire_load_model -name tsmc18_wl10 -library slow
```

Iran's Center for Integrated Circuits (ICIC)

Design Constraint Definition



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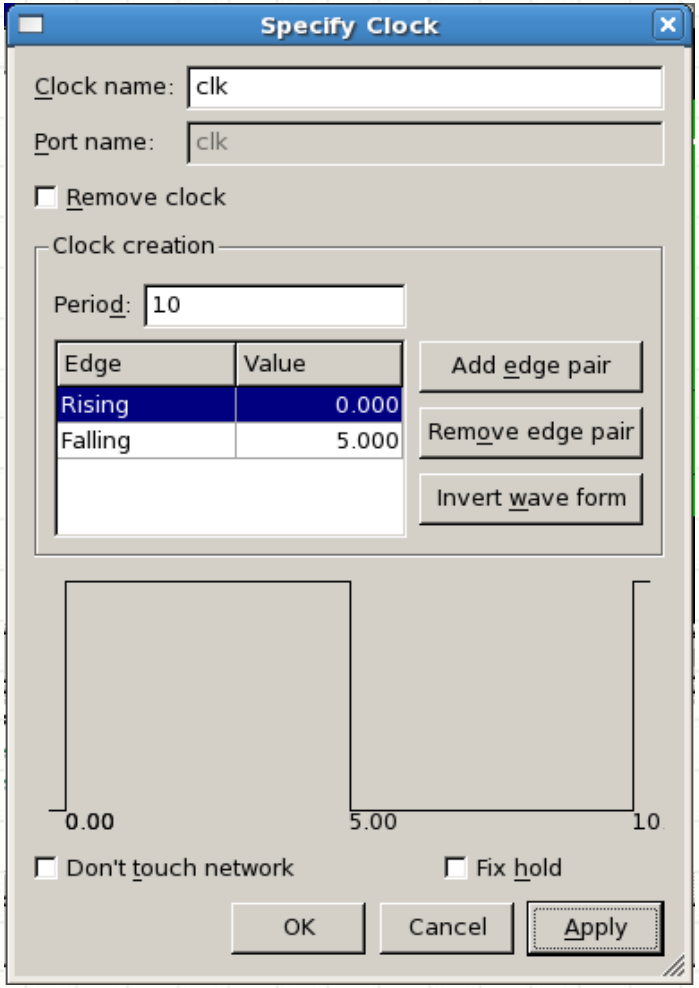
Design Constraint Definition

Attributes -> Specify Clock…

```
create_clock -name "clk"
 -period 10 -waveform {0 5}{ clk }
```



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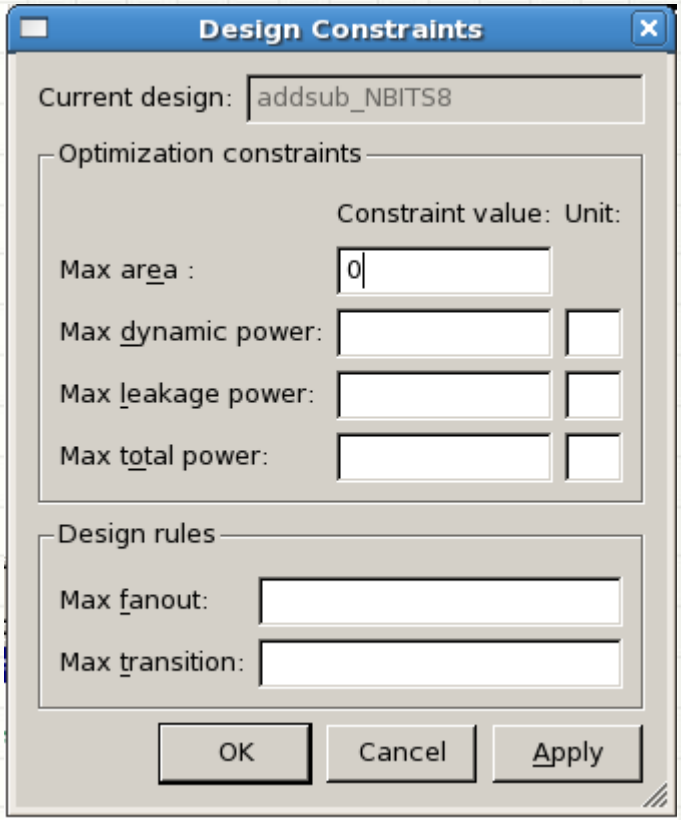
Design Constraint Definition

Attributes -> Optimization Constraints -> Design Constraints…

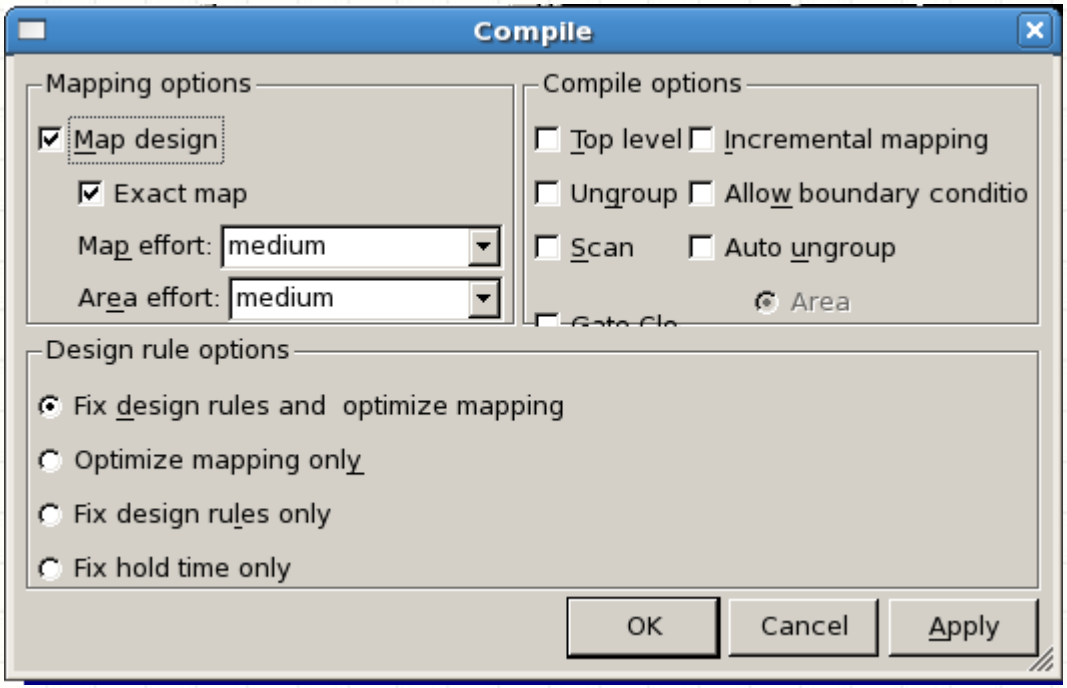
```
set_max_area 0
```



Iran's Center for Integrated Circuits (ICIC)

Design Mapping and Optimization

Design -> Compile Ultra…




```
compile_ultra -map_effort medium -area_effort medium
```

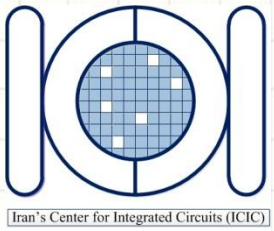
Iran's Center for Integrated Circuits (ICIC)

Report Generation and Outputs

Design -> Report Area…

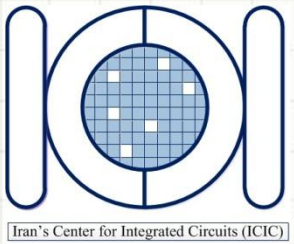
Timing -> Report Timing Path

```
write -hierarchy -format ddc -output ./out/addsub.ddc

write -hierarchy -format verilog -output ./out/addsub.v
```

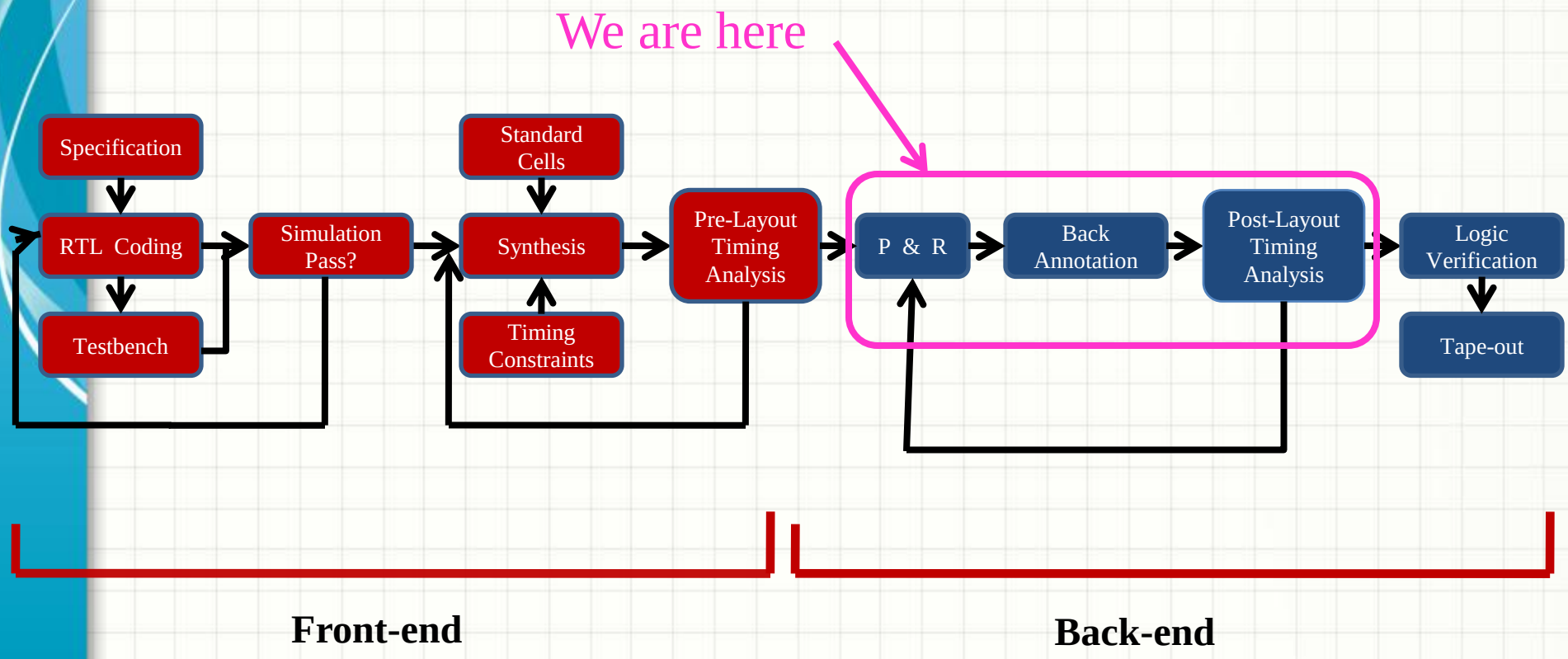


Standard Cell Placement and Routing

Cadence SOC Encounter



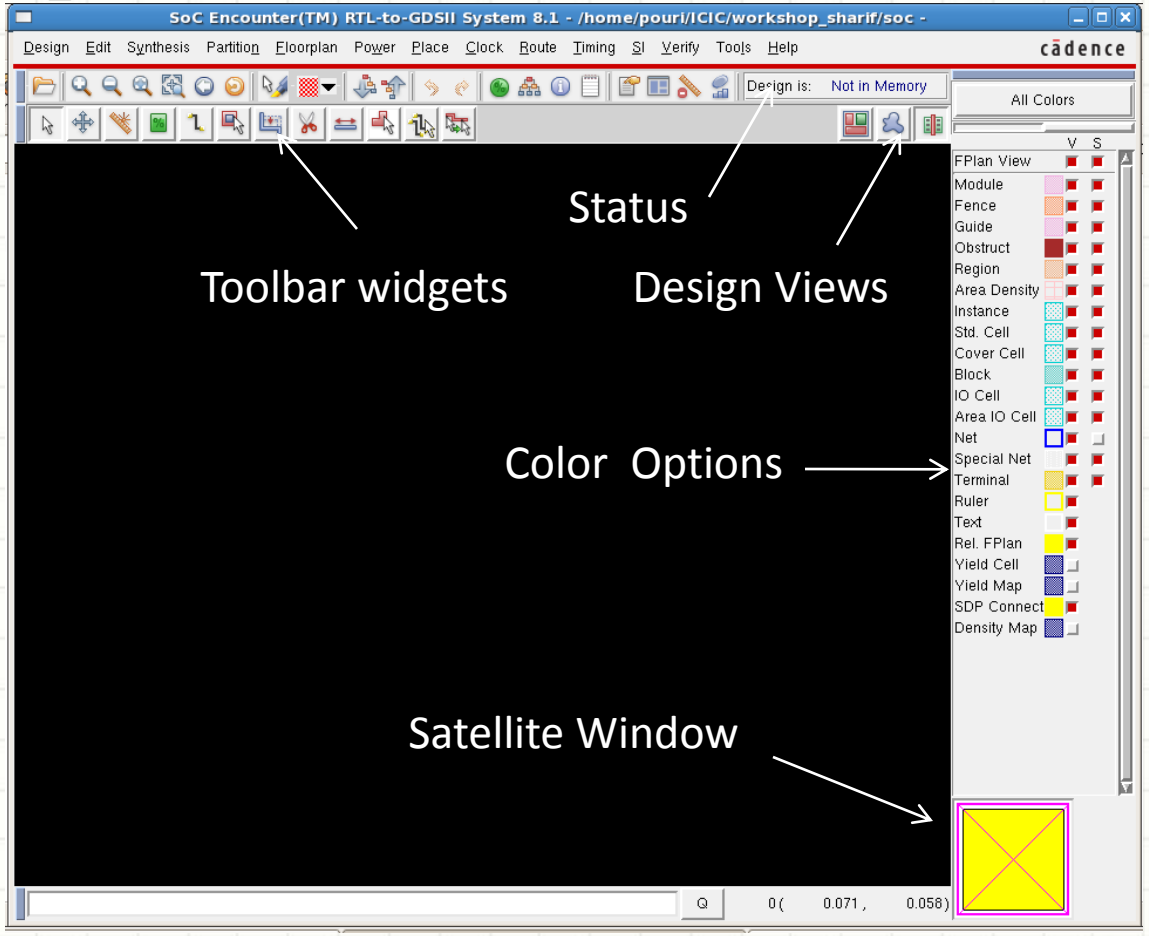
Digital Design Flow



Iran's Center for Integrated Circuits (ICIC)

Starting SOC Encounter

```
[user#@ICICHP home]$ cd digital_workshop/place_Route
[user#@ICICHP place_Route]$ encounter
```



Iran's Center for Integrated Circuits (ICIC)

Setting

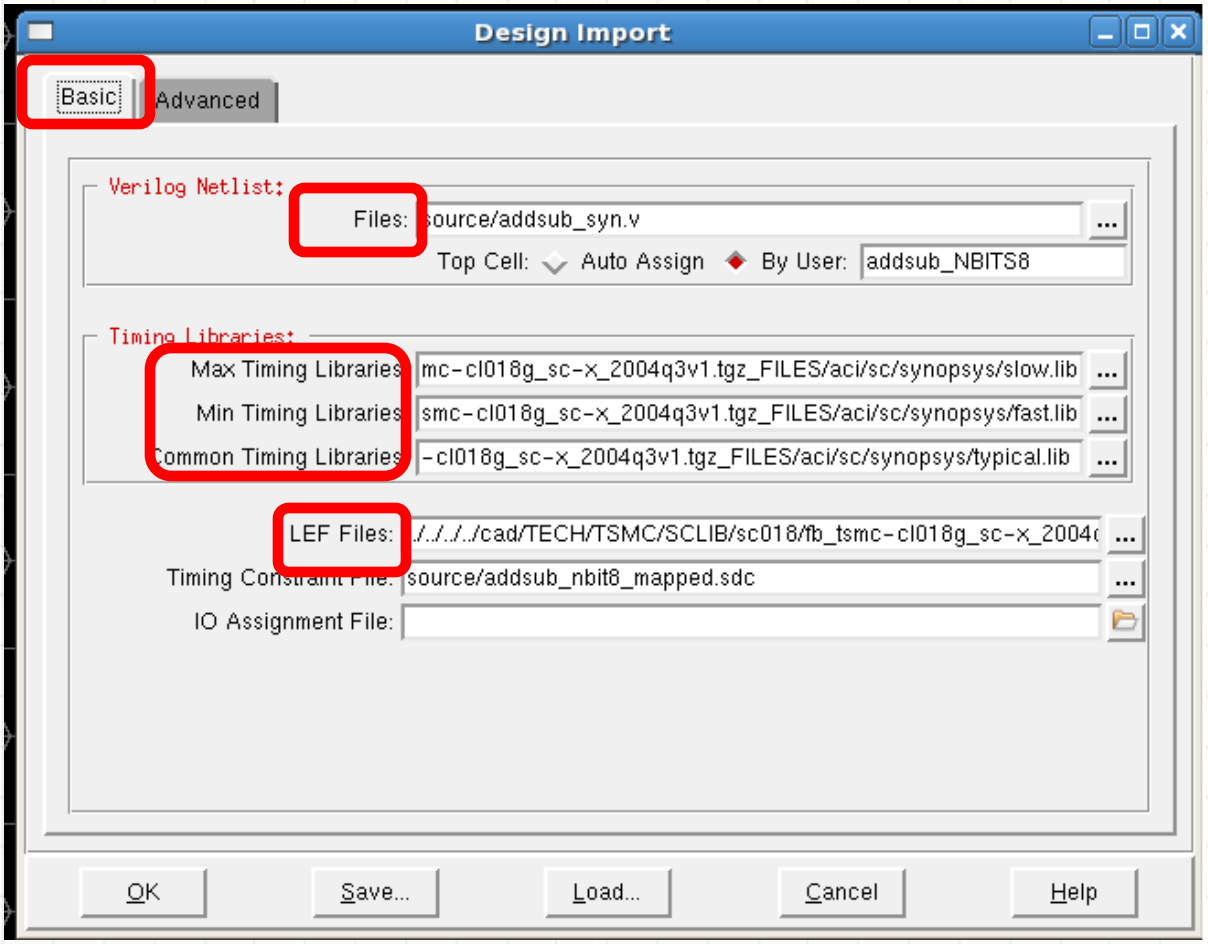
gedit source/addsub_NBITS8.conf

```
#####################################################
#                                   #
#  FirstEncounter Input configuration file     #
#                                   #
#####################################################
# Created by First Encounter v08.10-s338_1 on Sat Nov 12 12:31:56 2011
global rda_Input
set cwd /home/pouri/digital_workshop/place_Route
set rda_Input(import_mode) {-treatUndefinedCellAsBbox 0 -
    keepEmptyModule 1 -useLefDef56 1 }
```

Iran's Center for Integrated Circuits (ICIC)

Design Import

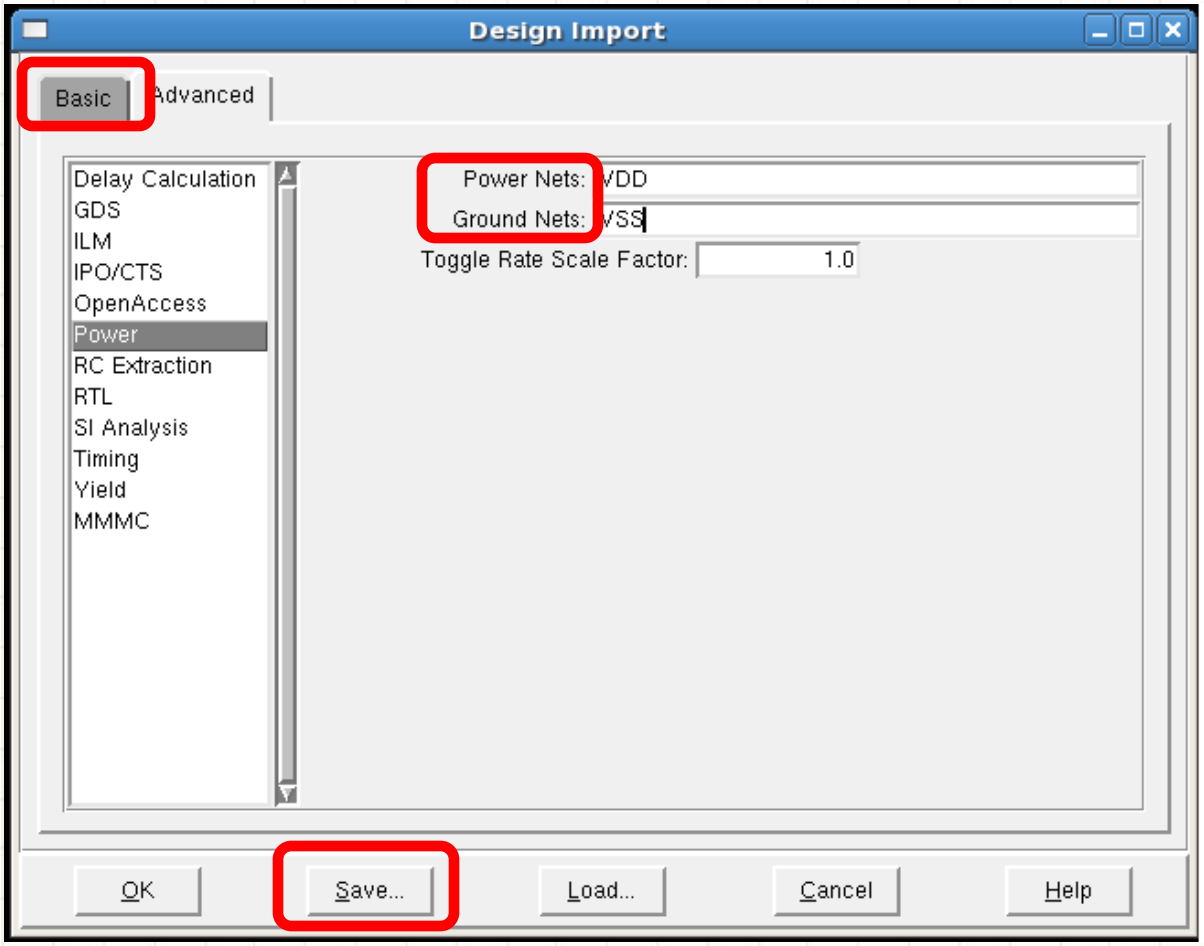
Design -> Design Import



Iran's Center for Integrated Circuits (ICIC)

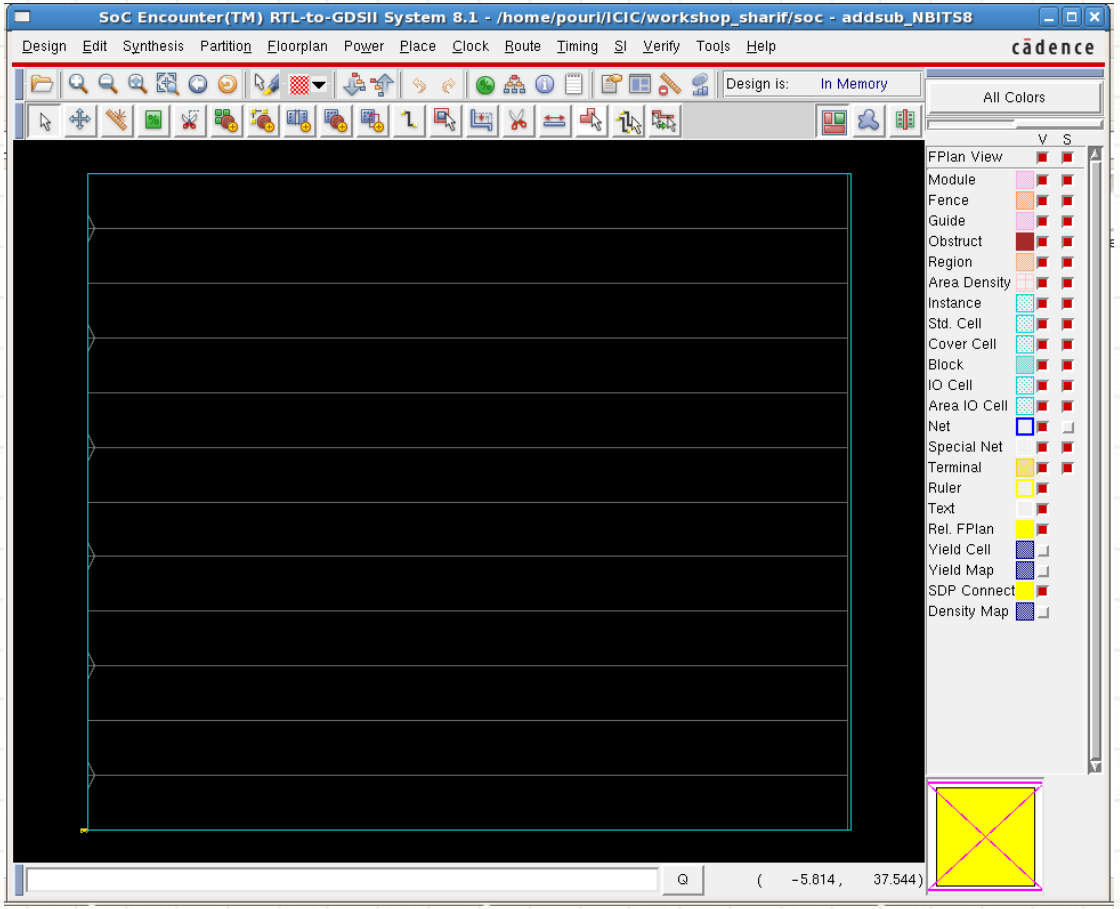
Design Import

Design -> Design Import



Iran's Center for Integrated Circuits (ICIC)

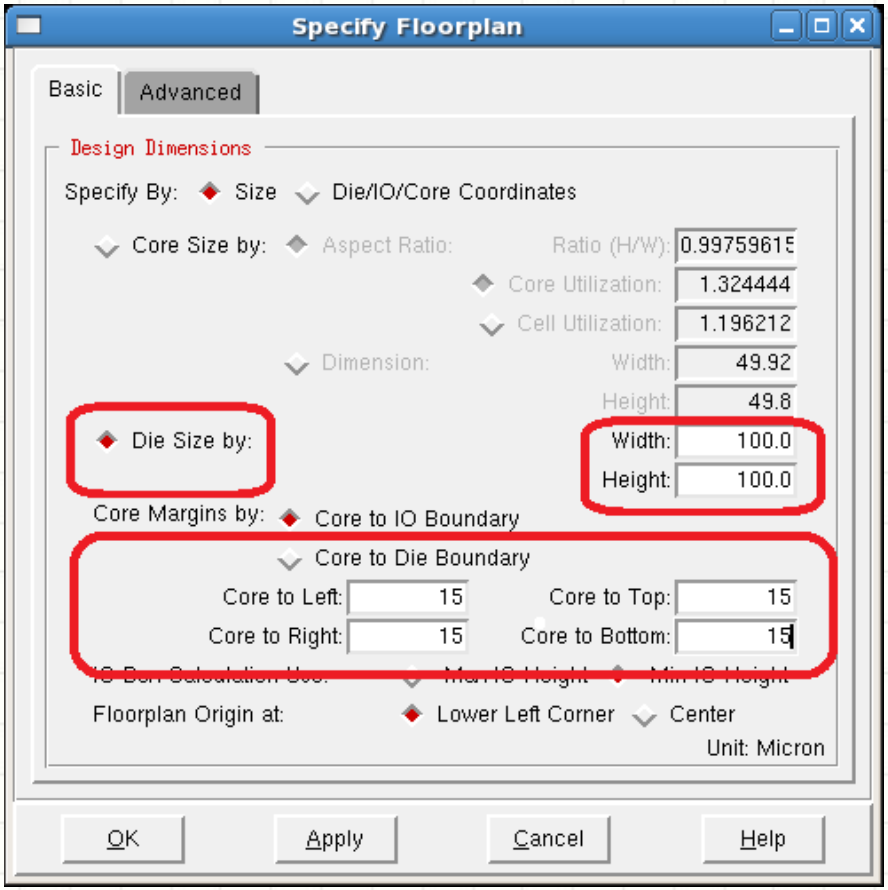
Design Import



Iran's Center for Integrated Circuits (ICIC)

Floorplan Specification

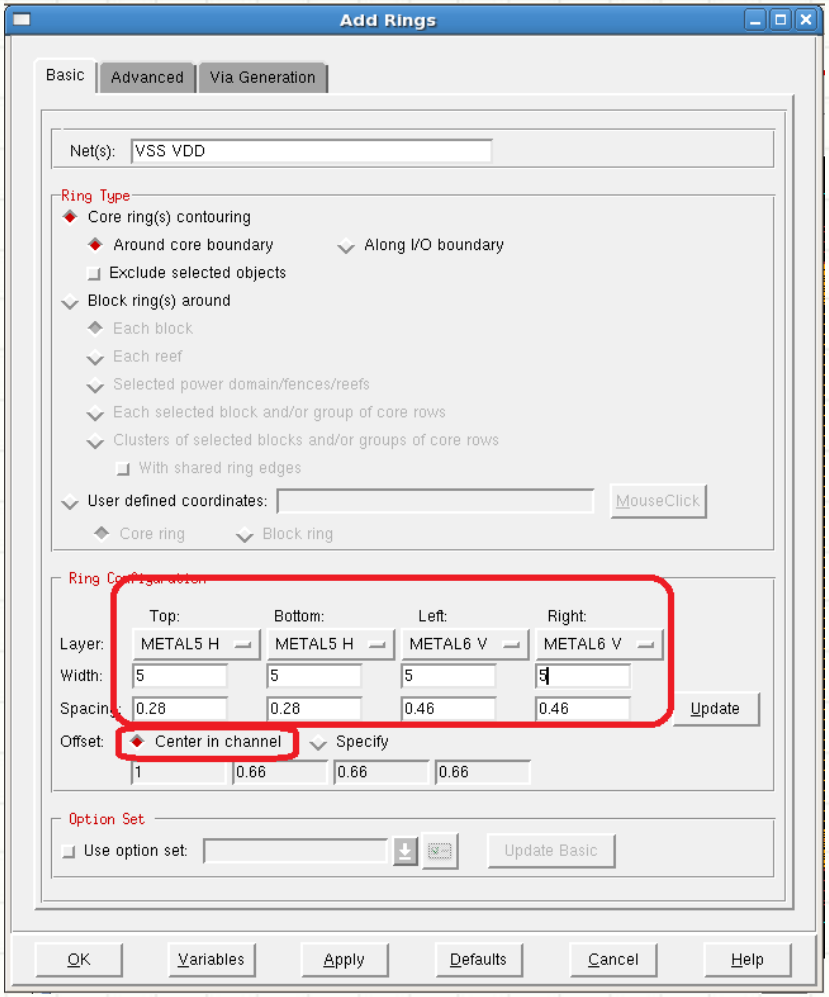
Floorplan -> Specify Floorpaln



Iran's Center for Integrated Circuits (ICIC)

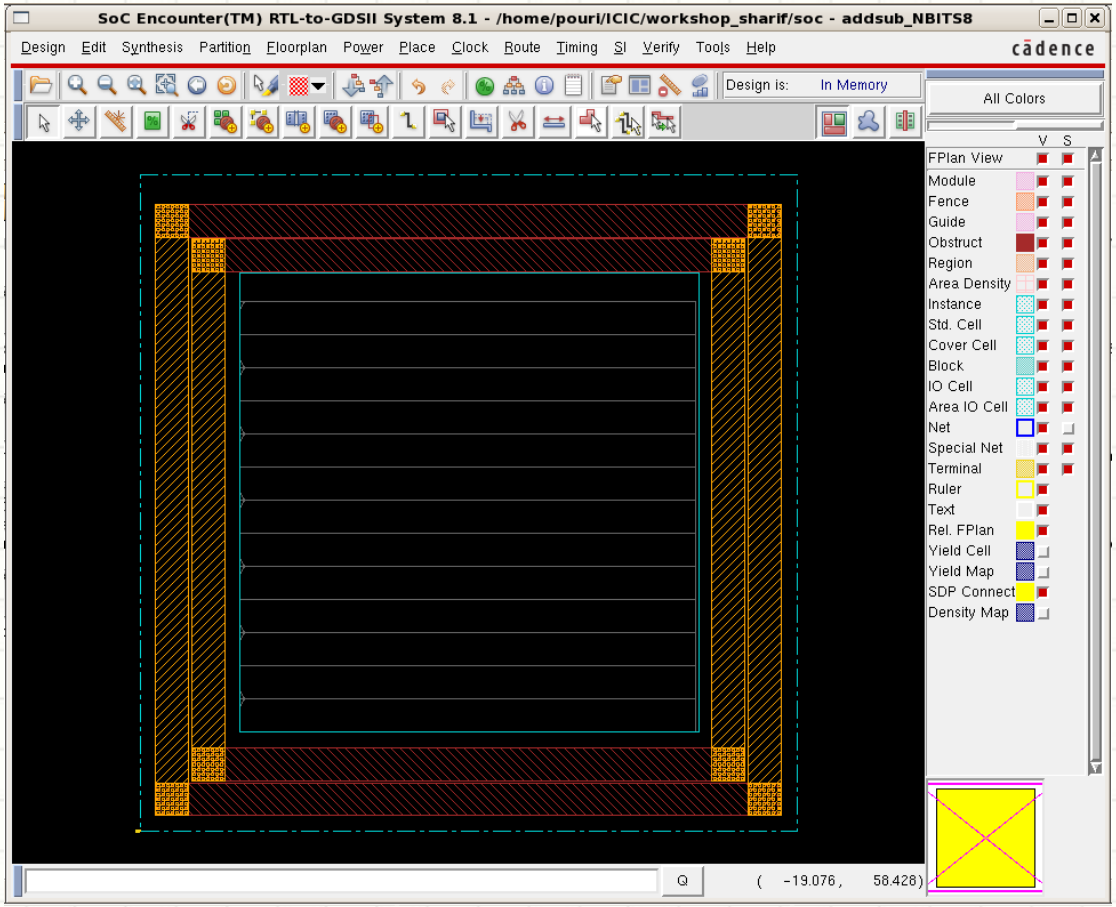
Power Planning- Add Rings

Power -> Power Planning -> Add Rings



Iran's Center for Integrated Circuits (ICIC)

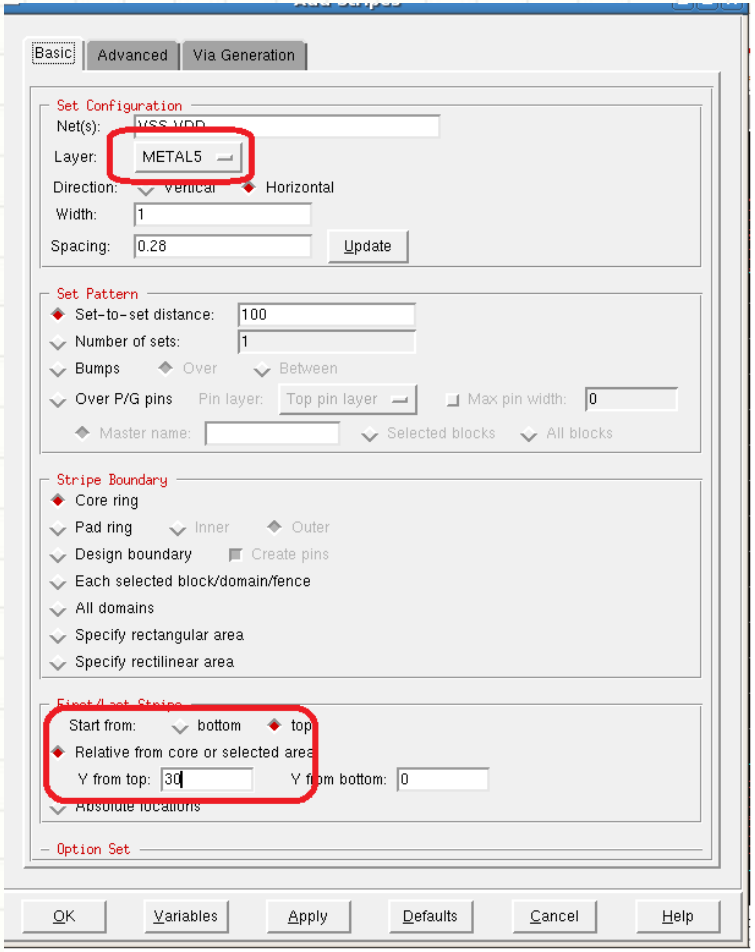
Power Planning- Add Rings



Iran's Center for Integrated Circuits (ICIC)

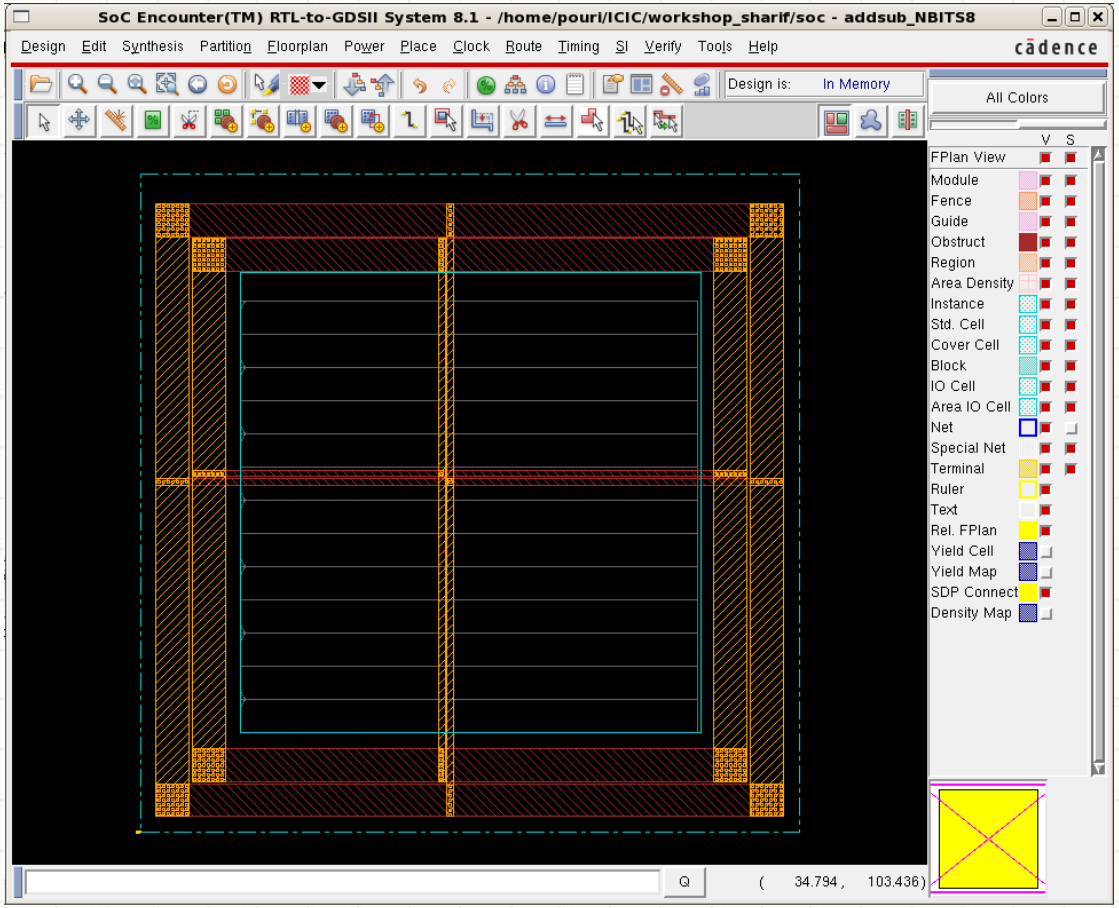
Power Planning- Add Stripes

Power -> Power Planning -> Add Stripes



Iran's Center for Integrated Circuits (ICIC)

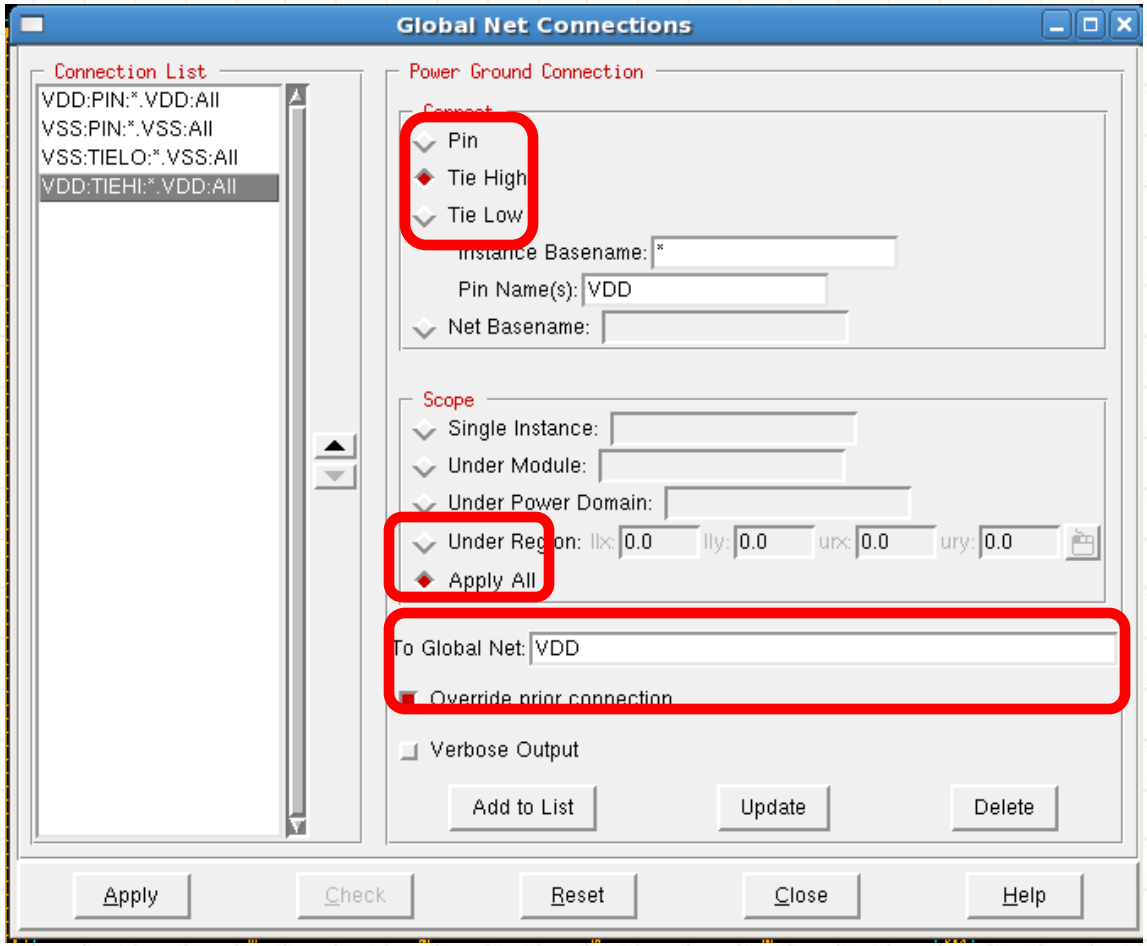
Power Planning- Add Stripes



Iran's Center for Integrated Circuits (ICIC)

Global Net Connection

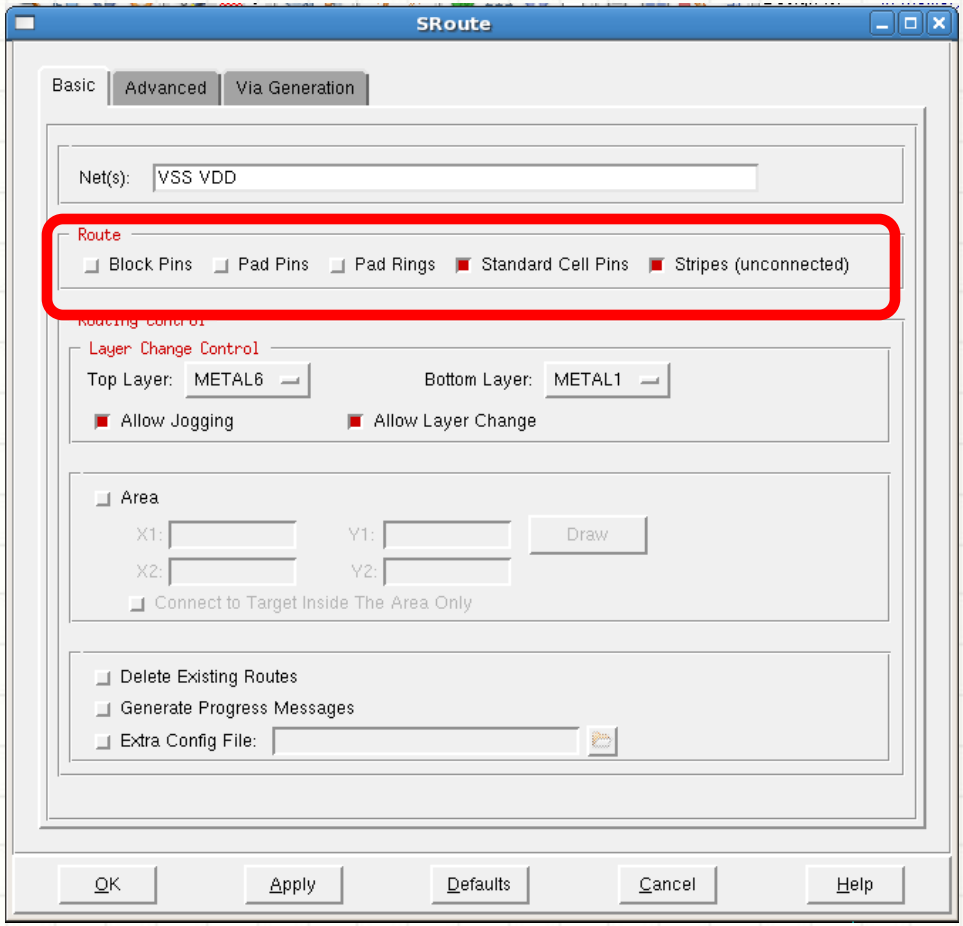
Floorplan -> Connect Global Nets



Iran's Center for Integrated Circuits (ICIC)

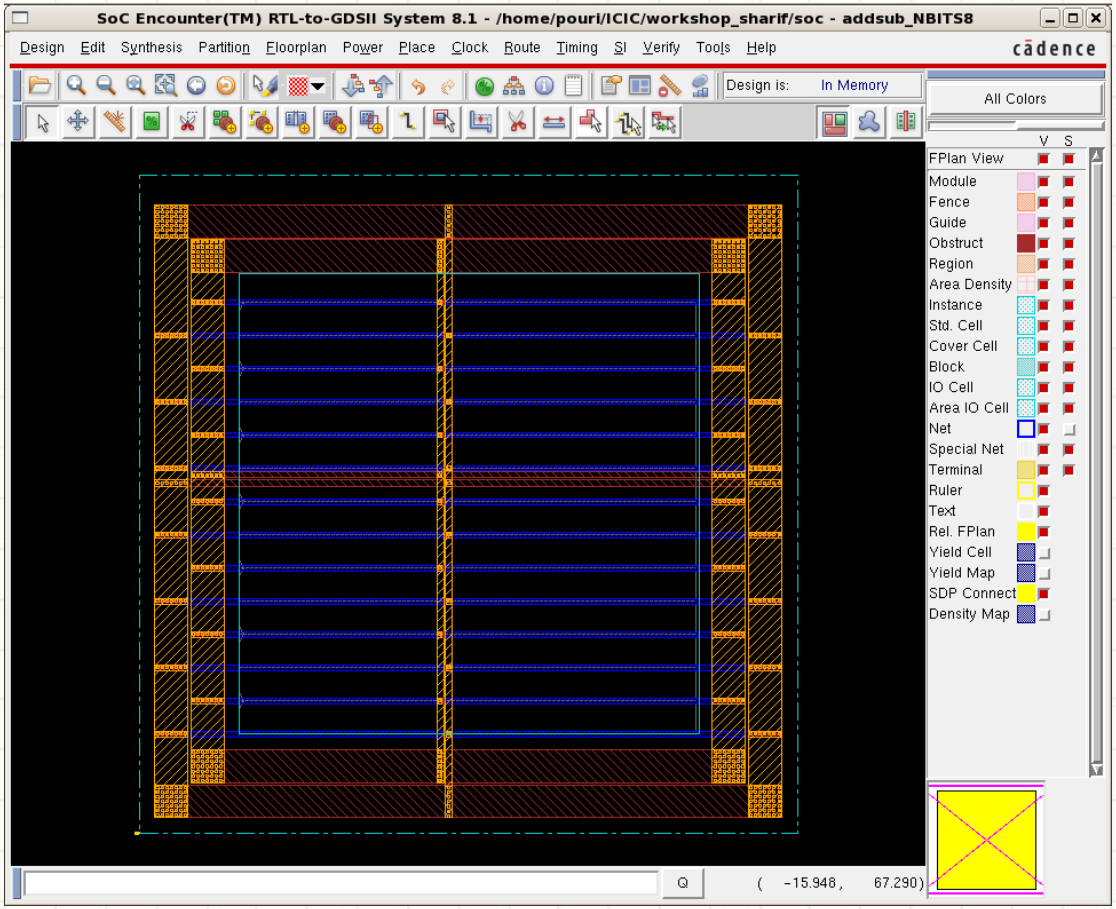
Sroute

Route -> Special Route…



Iran's Center for Integrated Circuits (ICIC)

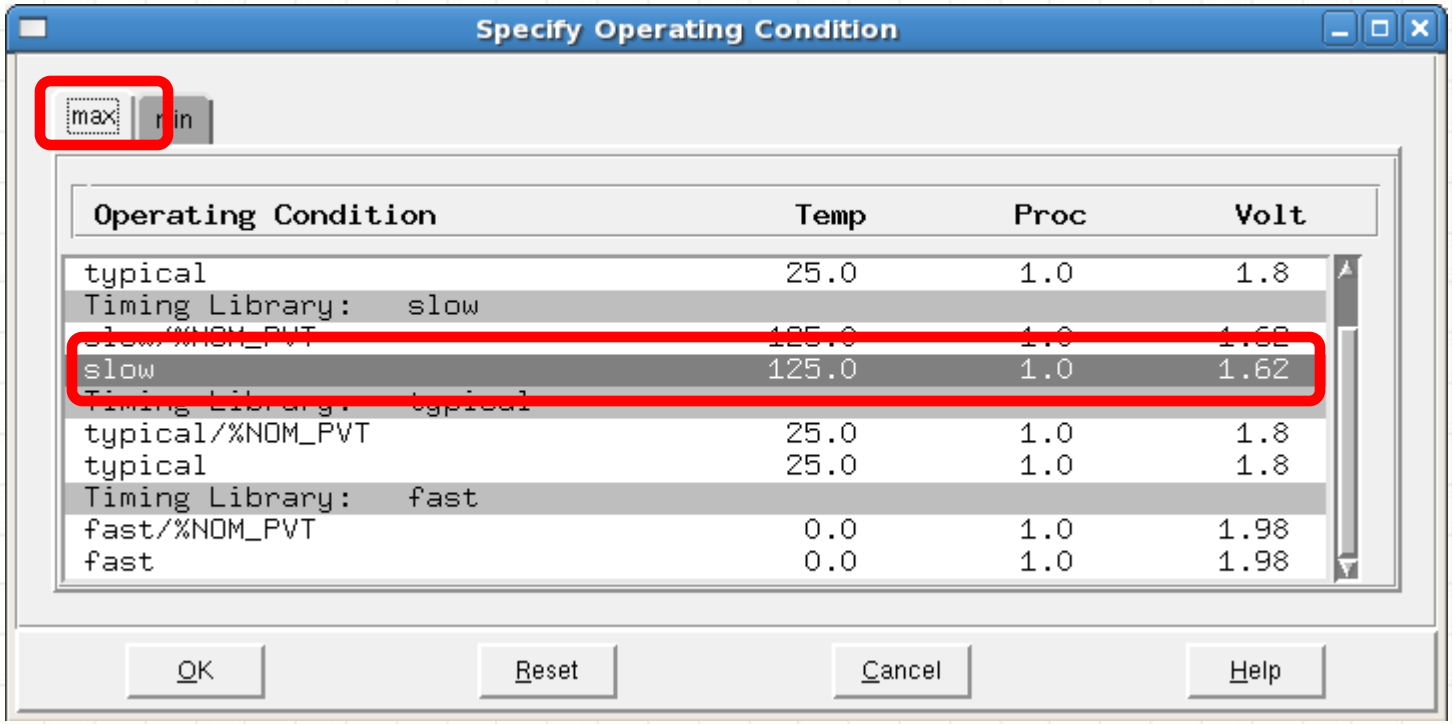
Sroute



Iran's Center for Integrated Circuits (ICIC)

Operating Conditions Definition

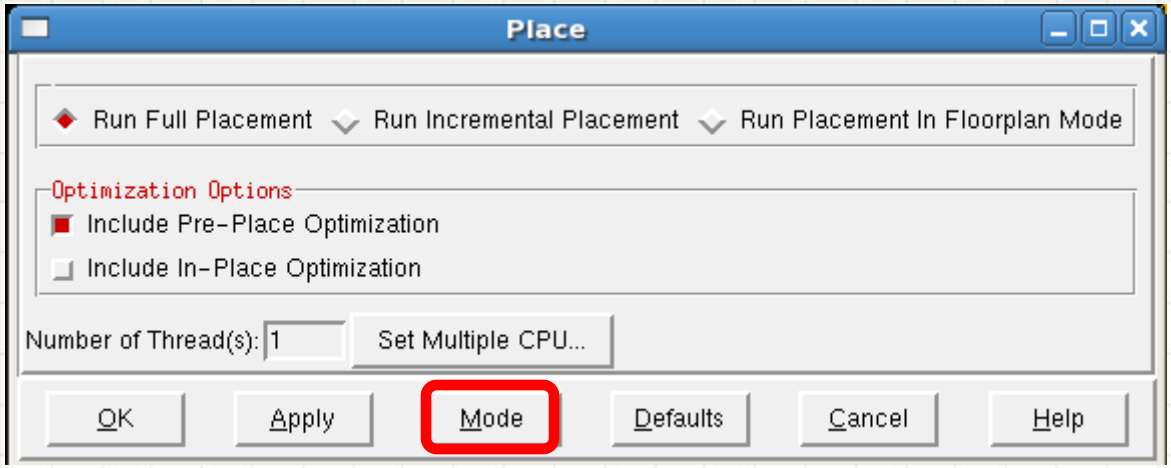
Timing -> Analysis Condition -> Specify Operating Condition/PVT…



Iran's Center for Integrated Circuits (ICIC)

Core Cell Placement

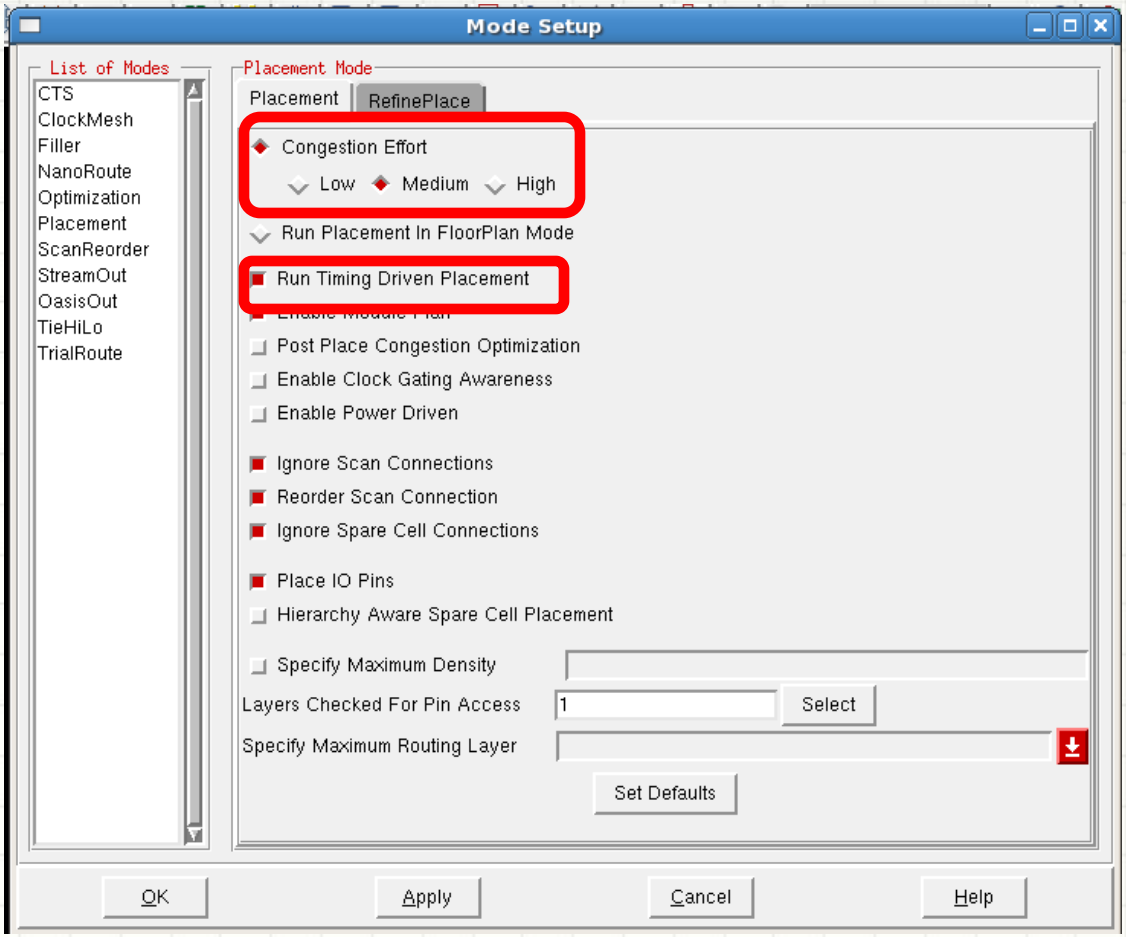
Place -> Standard Cells…



Iran's Center for Integrated Circuits (ICIC)

Core Cell Placement

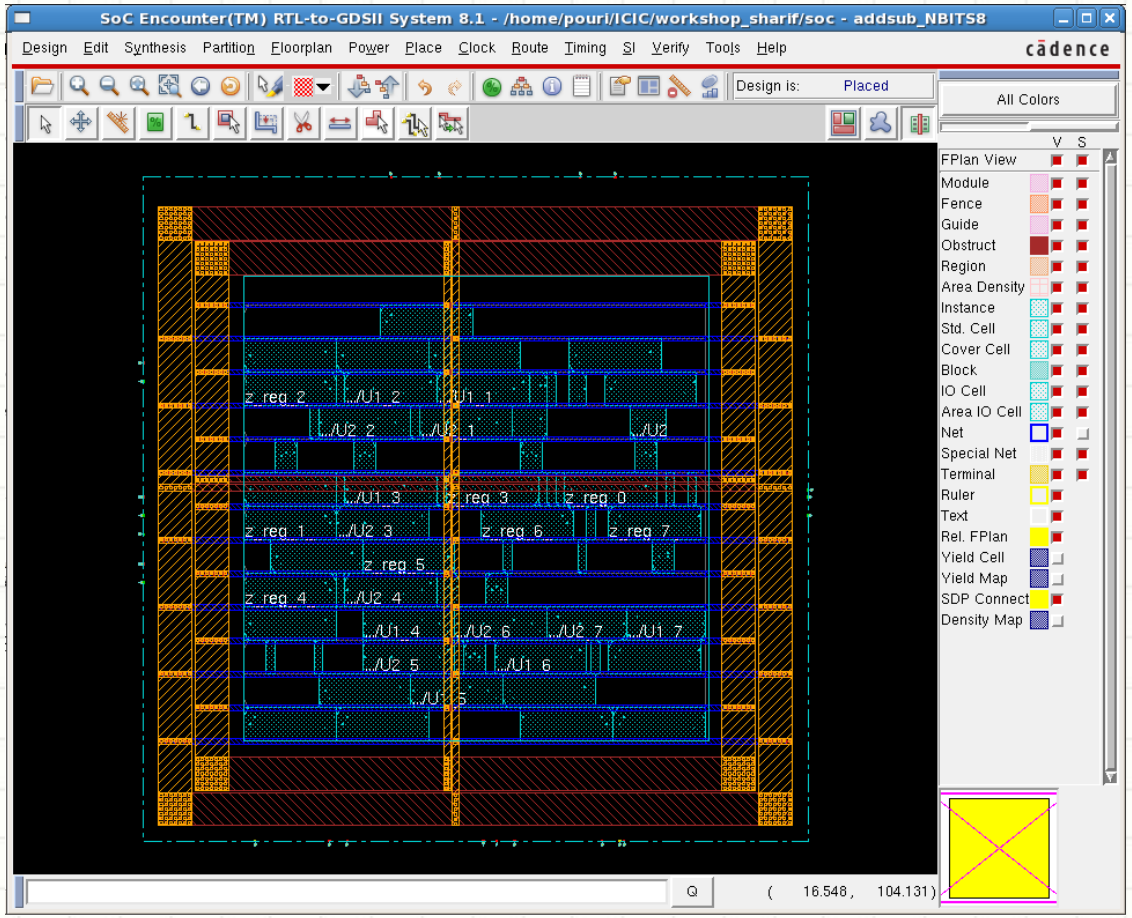
Place -> Standard Cells…-> Mode



Iran's Center for Integrated Circuits (ICIC)

Core Cell Placement

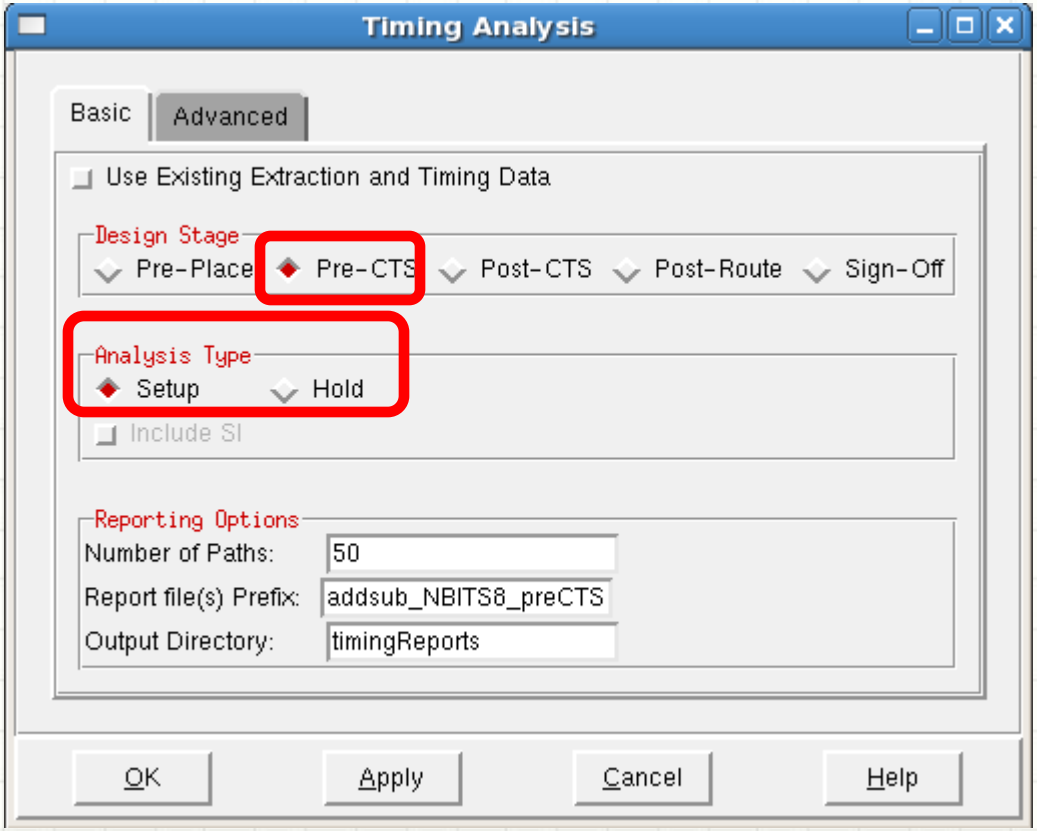
Design -> Save Design As … -> SoCE



Iran's Center for Integrated Circuits (ICIC)

Post-Placement Timing Analysis

Timing -> Analyze Timing…



Iran's Center for Integrated Circuits (ICIC)

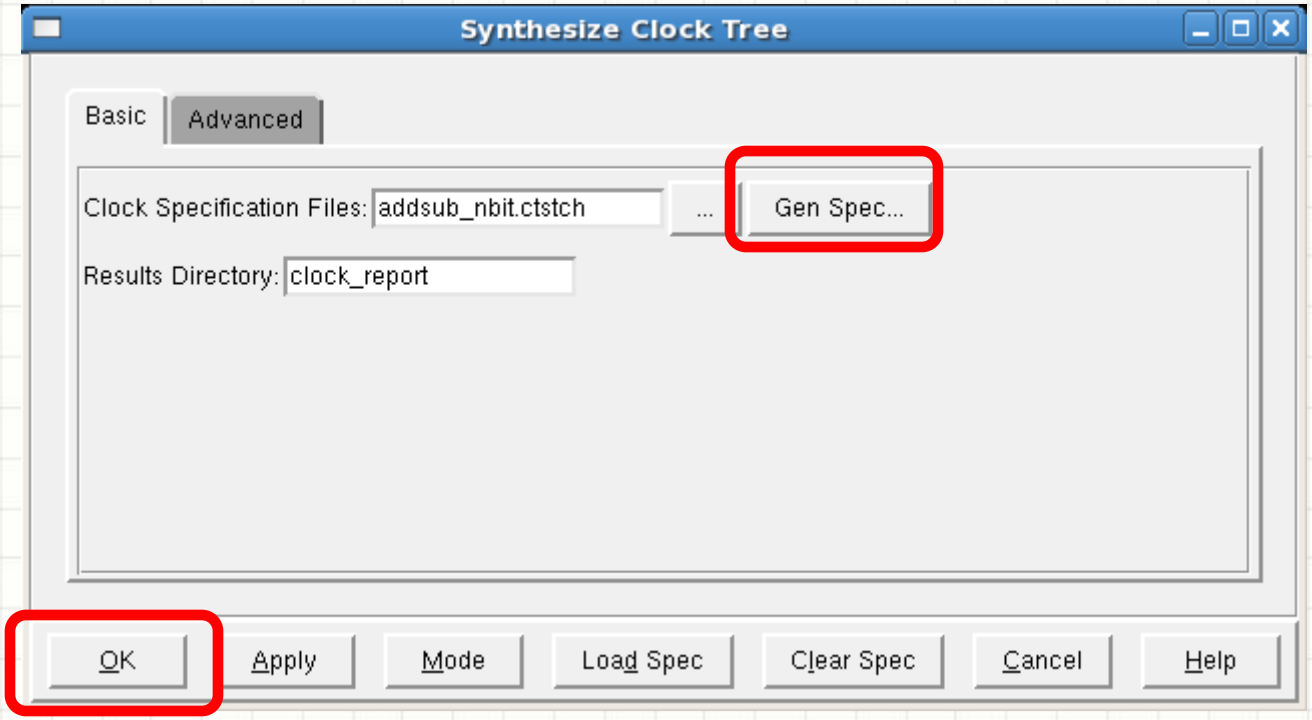
Post-Placement Timing Analysis

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | clkgate |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  6.042  |  6.042  |  9.034  |   N/A   |   N/A   |   N/A   |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |   N/A   |   N/A   |   N/A   |
|    Violating Paths:|    0    |    0    |    0    |   N/A   |   N/A   |   N/A   |
|          All Paths:|   48    |    8    |   48    |   N/A   |   N/A   |   N/A   |
+--------------------+---------+---------+---------+---------+---------+---------+

+-----------------+--------------------------------+-------------------+
|                 |              Real              |       Total       |
|    DRVs         +------------------+-------------+-------------------|
|                 |  Nr nets(terms)  | Worst Vio   |  Nr nets(terms)   |
+-----------------+------------------+-------------+-------------------+
|   max_cap       |      0 (0)       |   0.000     |      0 (0)        |
|   max_tran      |      0 (0)       |   0.000     |      0 (0)        |
|   max_fanout    |      0 (0)       |     0       |      0 (0)        |
+-----------------+------------------+-------------+-------------------+
```

Iran's Center for Integrated Circuits (ICIC)

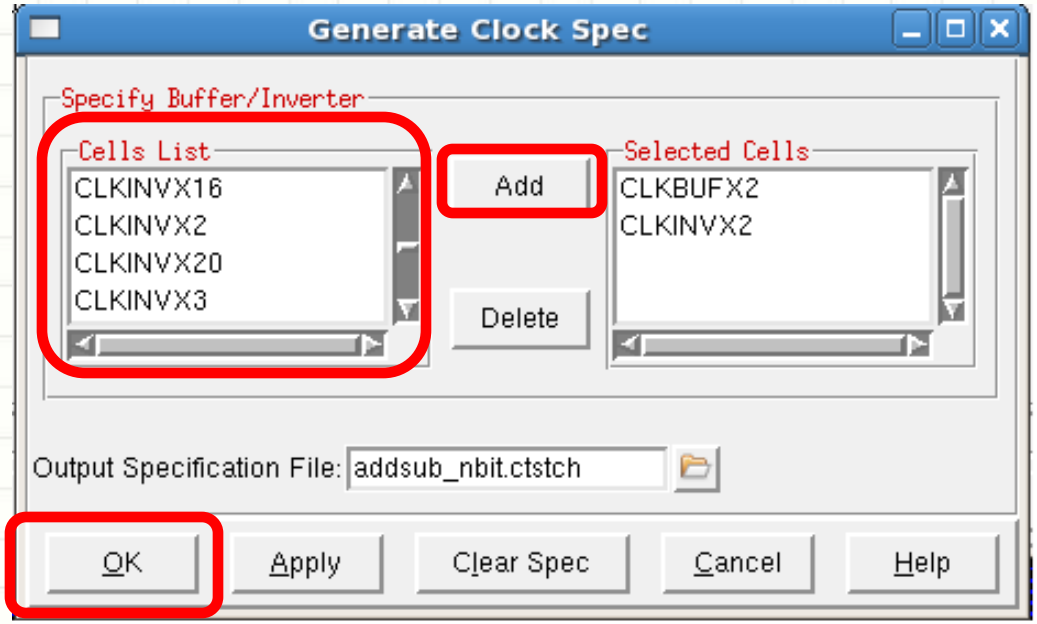
Clock Tree Synthesis

Clock -> Design Clock…



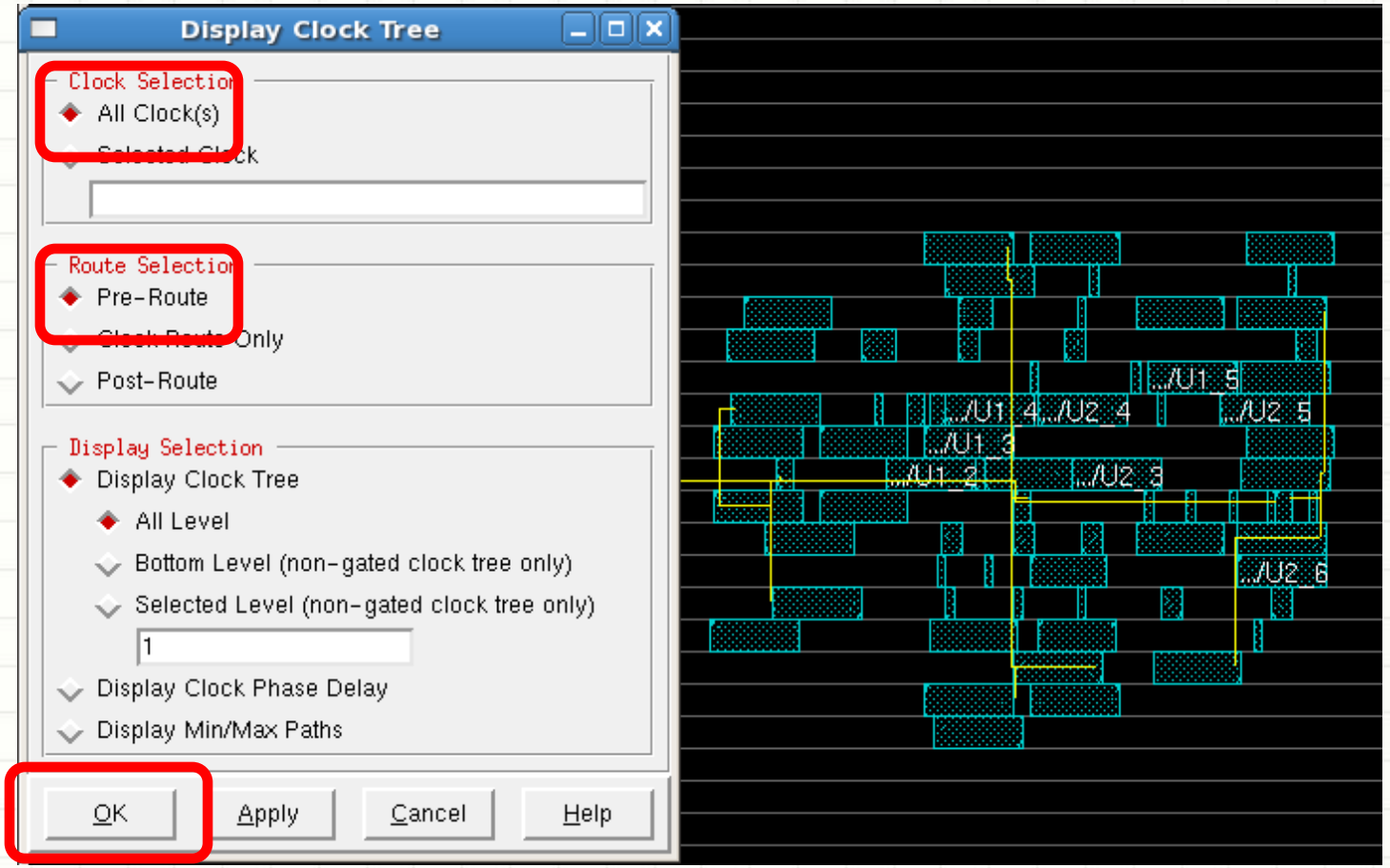
Iran's Center for Integrated Circuits (ICIC)

Clock Tree Synthesis



Iran's Center for Integrated Circuits (ICIC)

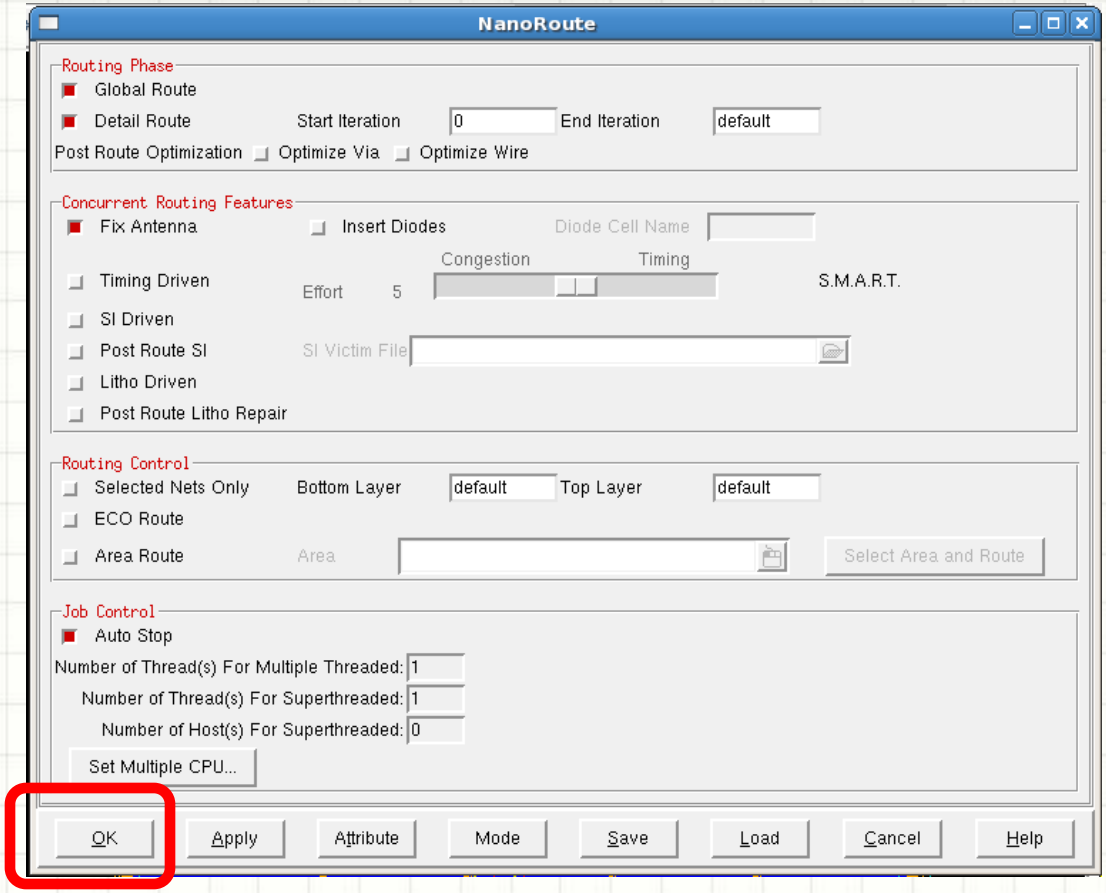
Clock Tree Synthesis



Iran's Center for Integrated Circuits (ICIC)

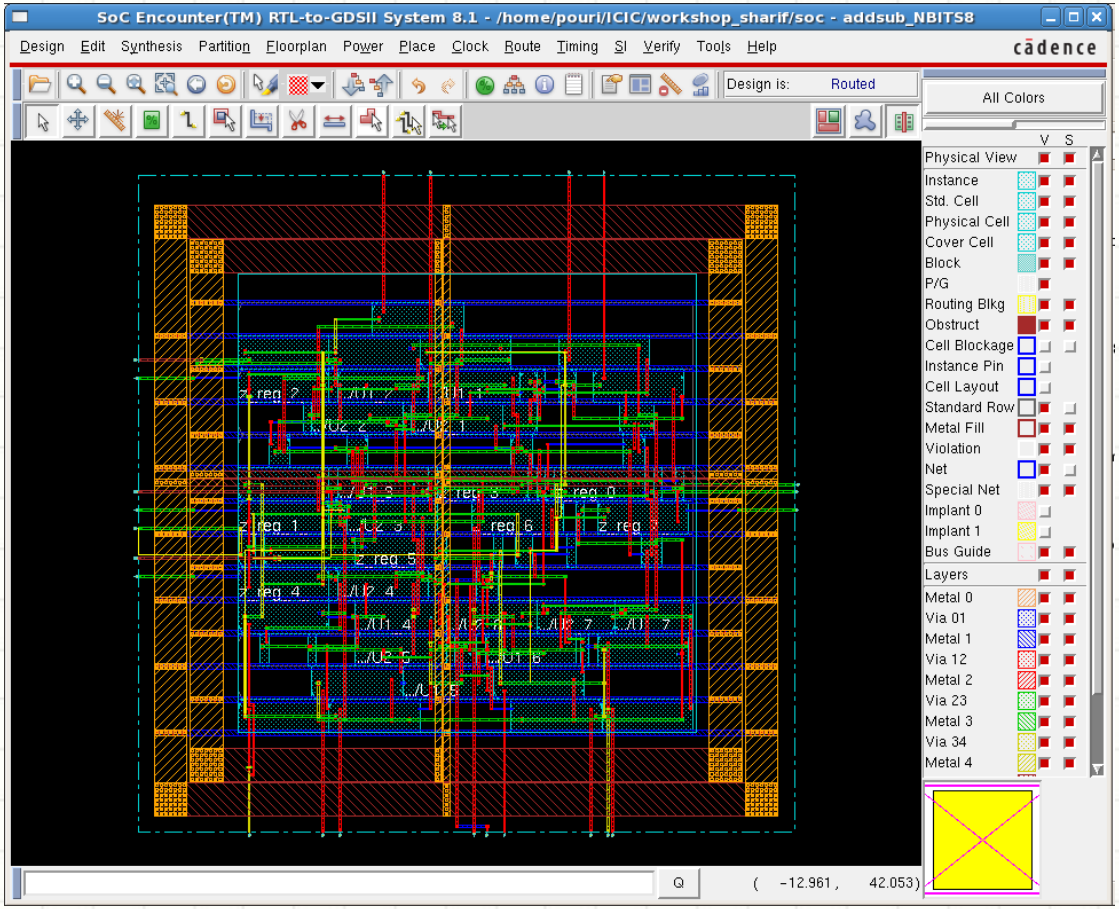
Design Routing

Route -> NanoRoute -> Route



Iran's Center for Integrated Circuits (ICIC)

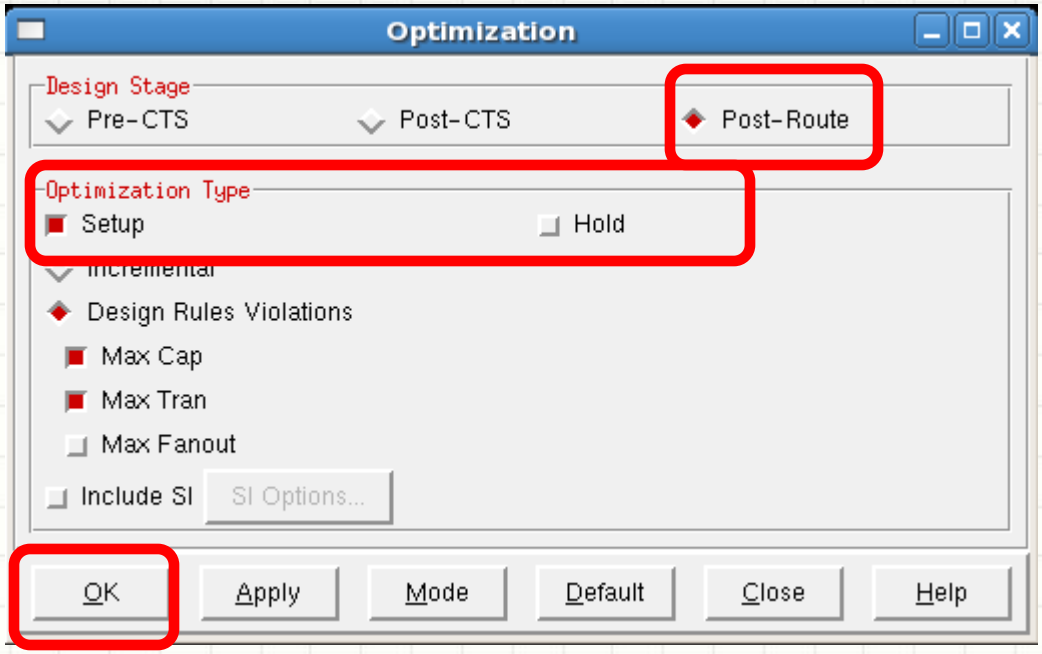
Design Routing



Iran's Center for Integrated Circuits (ICIC)

Post-Routing Timing Optimization and Analysis

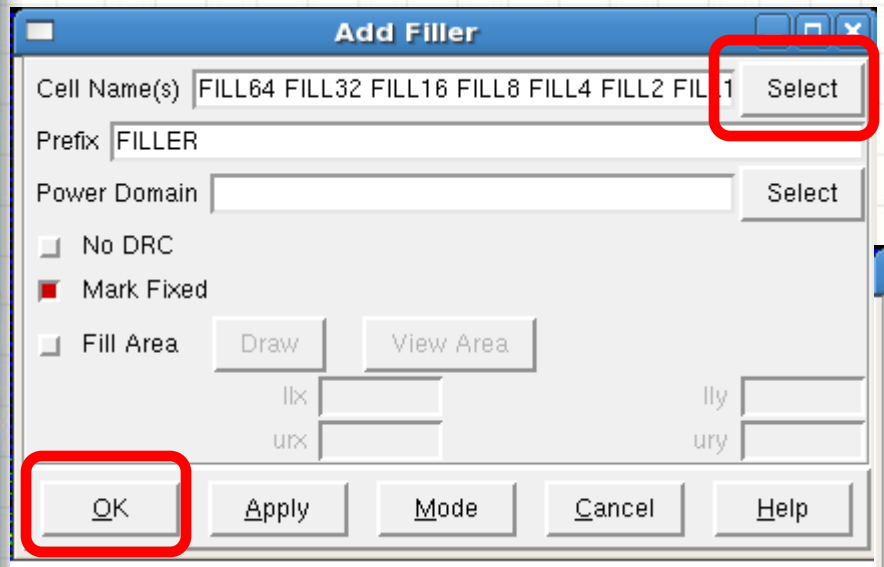
Timing -> Optimize…

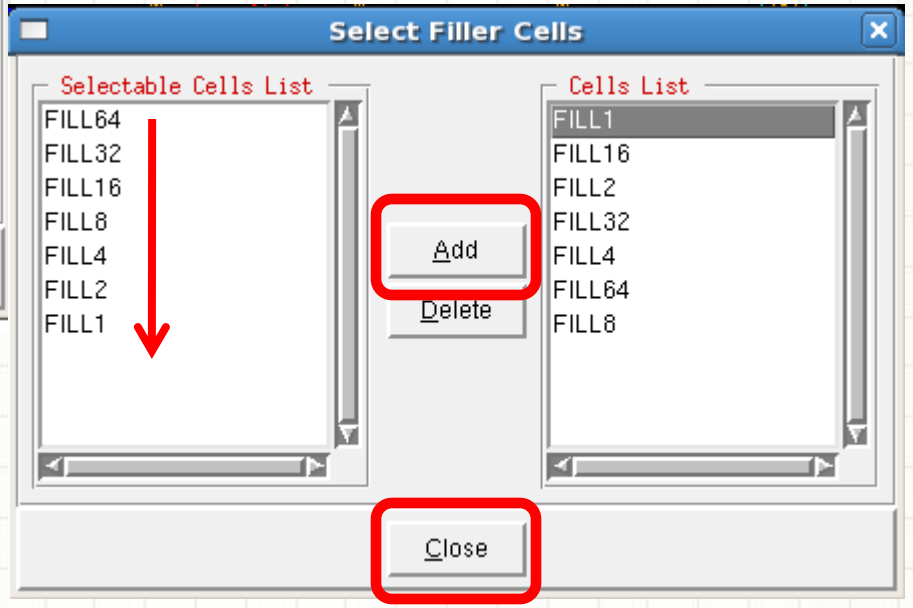


Iran's Center for Integrated Circuits (ICIC)

Filler Cell Placement

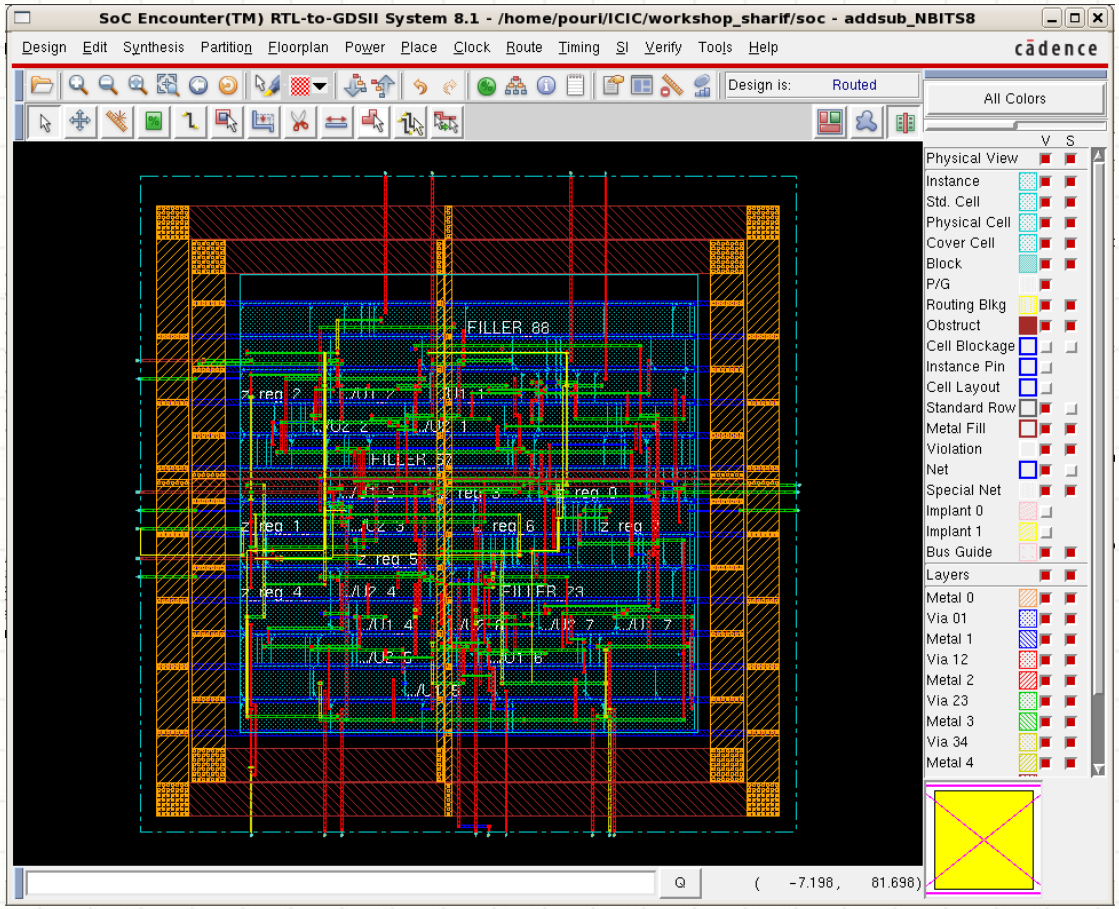
Place -> Physical Cells -> Add Filler…





Iran's Center for Integrated Circuits (ICIC)

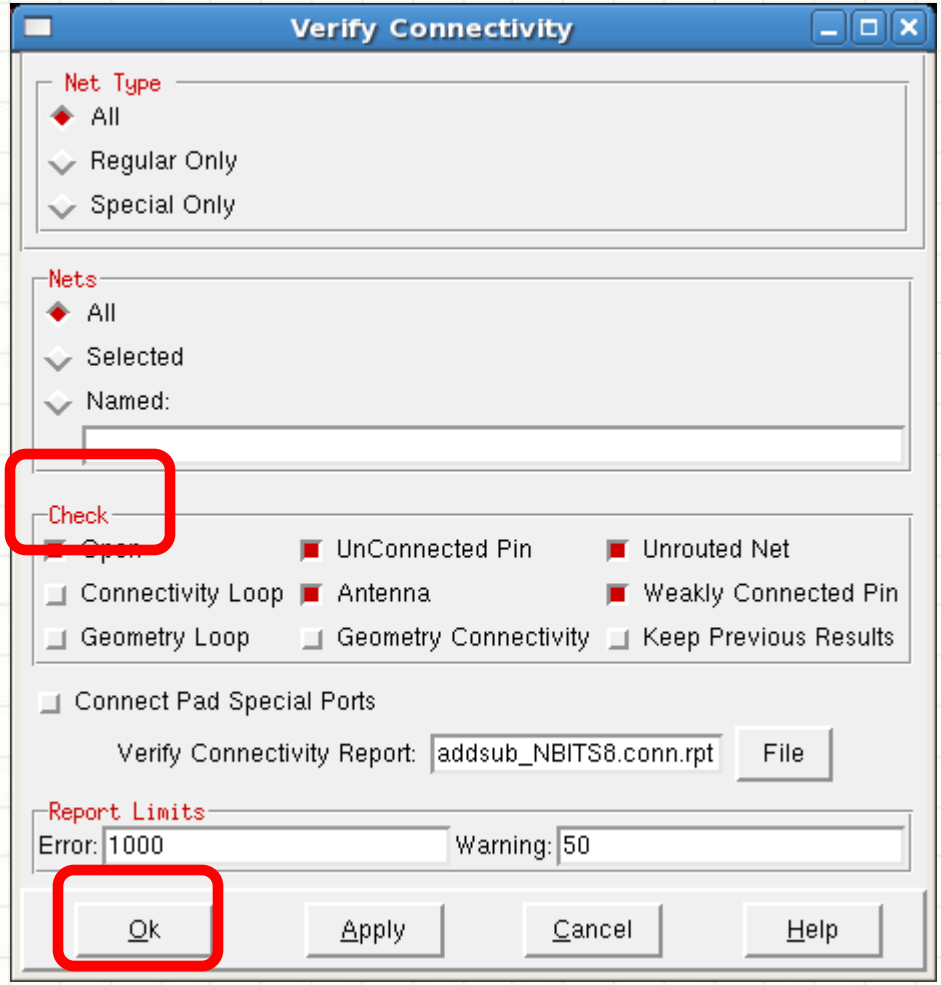
Filler Cell Placement



Iran's Center for Integrated Circuits (ICIC)

Design Checks

Verify -> Verify Connectivity…



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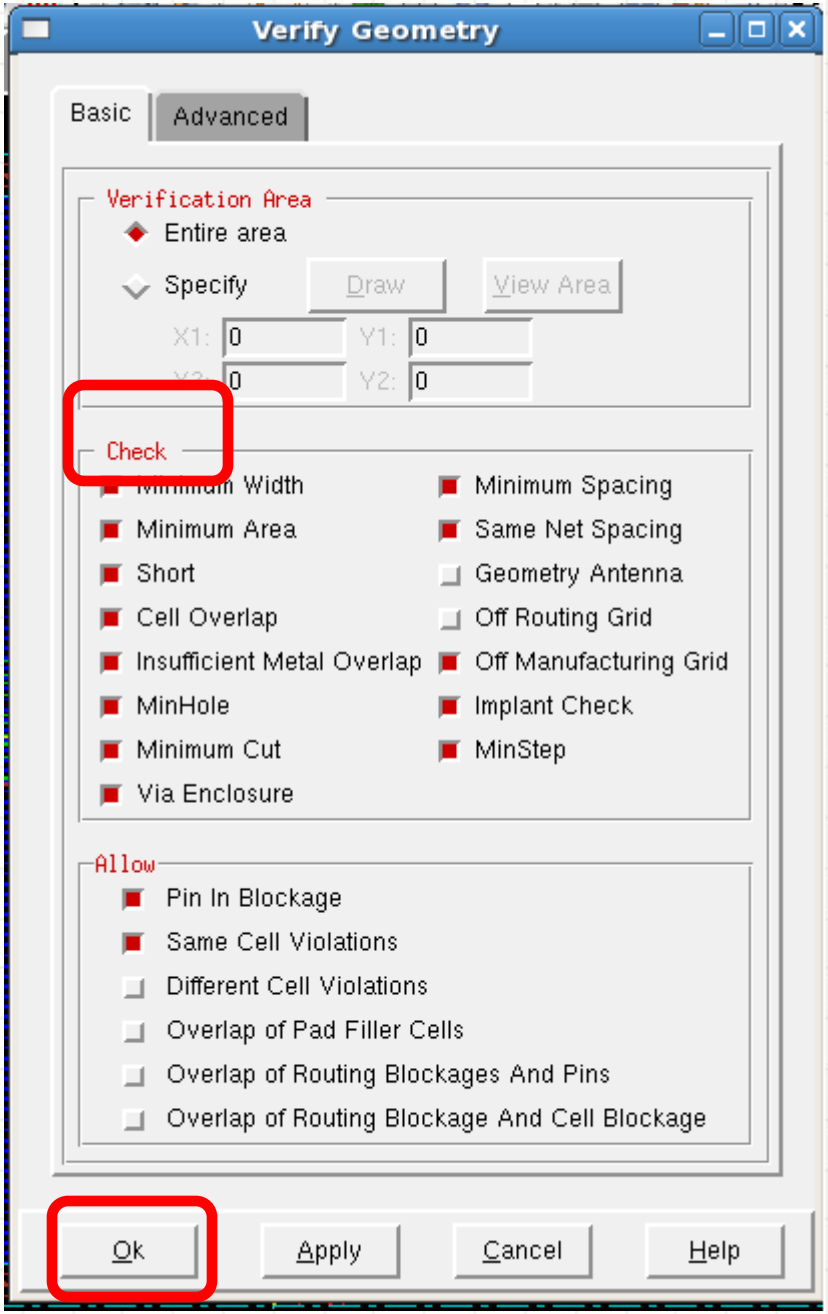
Design Checks

Verify -> Verify Geometry…



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Report Generation

Design -> Report -> Netlis Statistics…

```
encounter 1> *** Statistics for net list addsub_NBITS8 ***
Number of cells      = 1774
Number of nets       = 104
Number of tri-nets   = 0
Number of degen nets = 0
Number of pins       = 289
Number of i/os       = 27

Number of nets with    2 terms = 78 (75.0%)
Number of nets with    3 terms = 16 (15.4%)
Number of nets with    4 terms = 2 (1.9%)
Number of nets with    5 terms = 1 (1.0%)
Number of nets with    9 terms = 4 (3.8%)
Number of nets with >=10 terms = 3 (2.9%)

*** 17 Primitives used:
Primitive XOR3X2 (2 insts)
Primitive ADDFX2 (12 insts)
Primitive AND2X2 (1 insts)
Primitive AOI22X1 (8 insts)
Primitive CLKBUFX2 (4 insts)
Primitive DFFRHQX1 (24 insts)
Primitive INVX1 (19 insts)
Primitive OR2X2 (1 insts)
Primitive XNOR2X1 (1 insts)
Primitive XOR2X1 (1 insts)
Primitive FILL1 (40 insts)
Primitive FILL16 (120 insts)
Primitive FILL2 (41 insts)
Primitive FILL32 (28 insts)
Primitive FILL4 (136 insts)
Primitive FILL64 (1209 insts)
Primitive FILL8 (127 insts)
************
```

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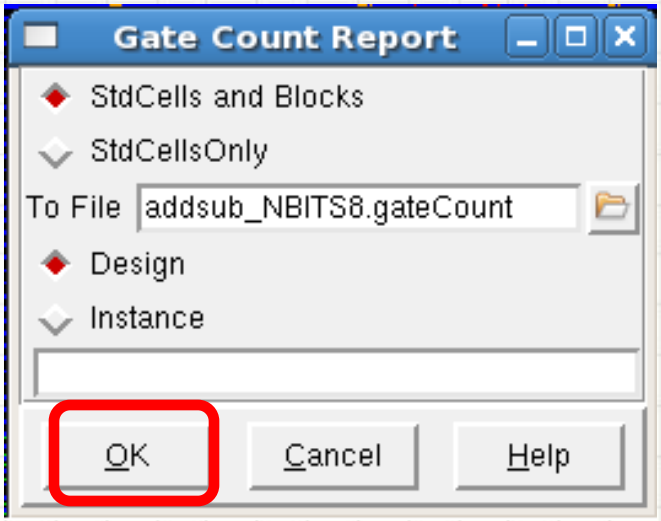
Report Generation

Design -> Report -> Gate Count…



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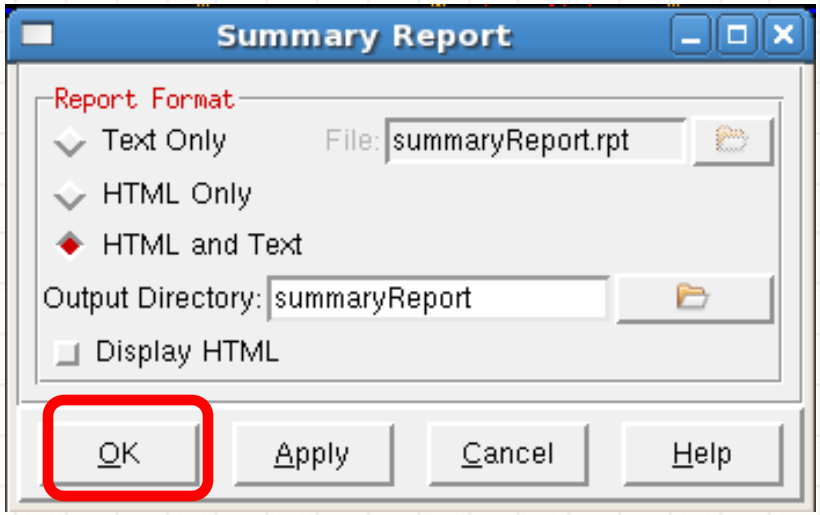
Report Generation

Design -> Report -> Summary…



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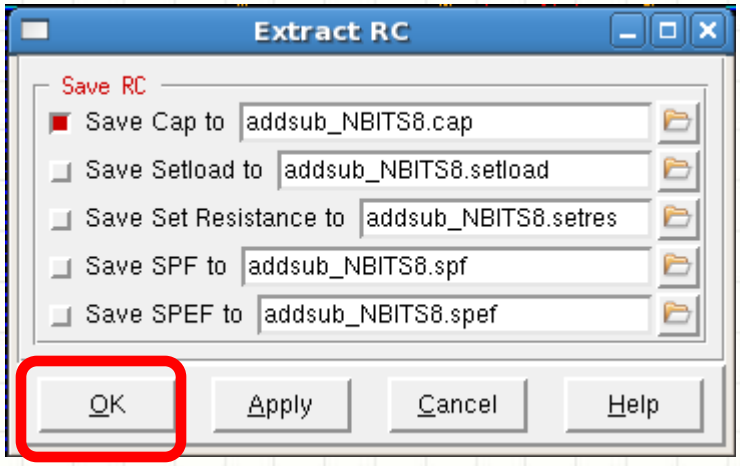
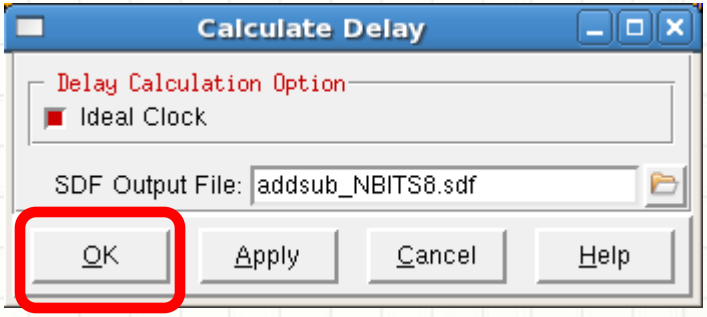
Post-Route Timing Data Extraction

Timing -> Extract RC…

Timing -> Calculate Delay…





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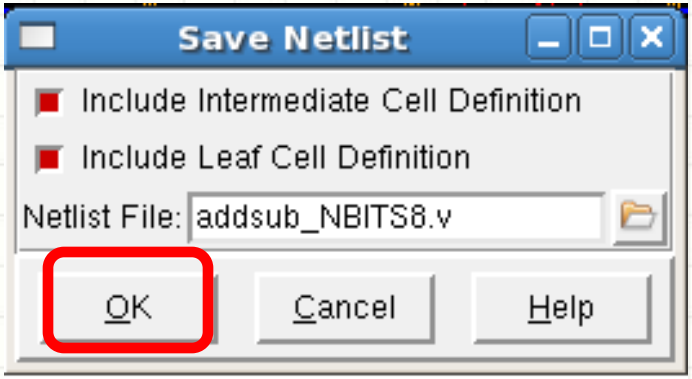
Post-Route Netlist Generation

Design -> Save -> Netlist



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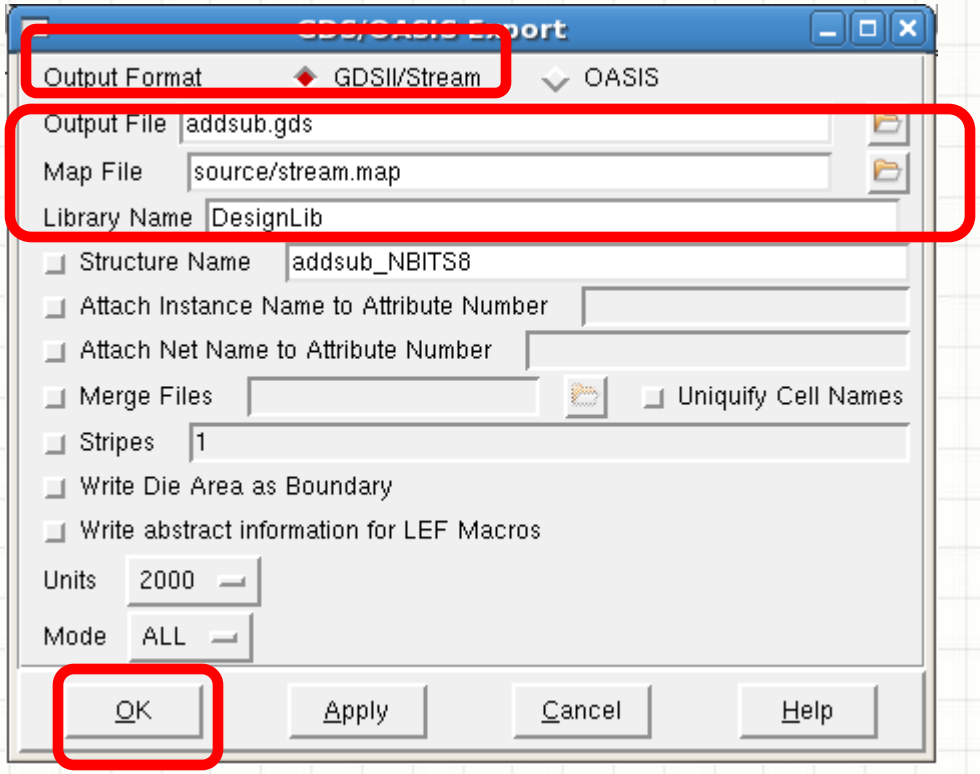
GDSII File Generation

Design -> Save -> GDS/OASIS



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Thanks For your Attention