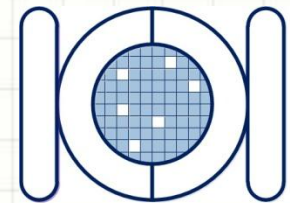


DIGITAL DESIGN FLOW

For EDA Tools:
Synopsys Design Compiler
Cadence SOC Encounter

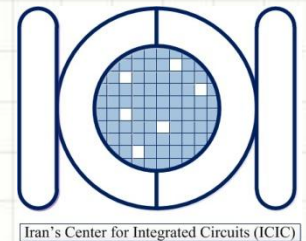
July 2012



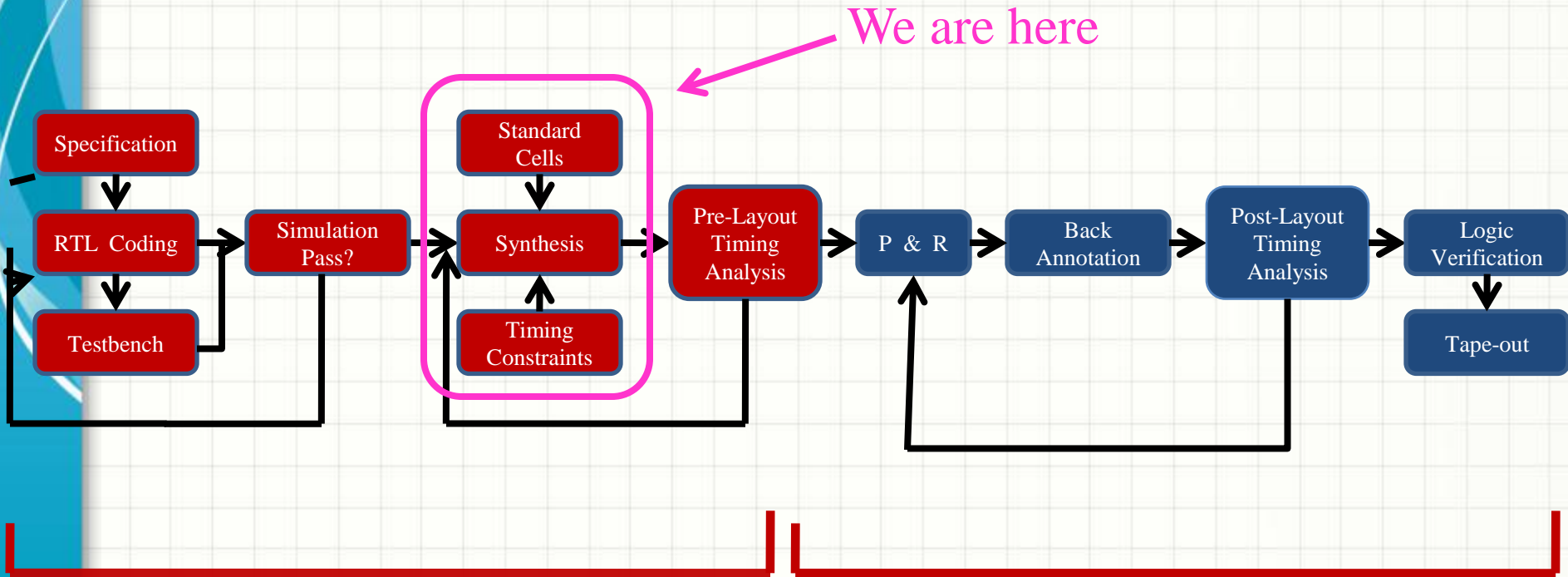
Iran's Center for Integrated Circuits (ICIC)

LOGIC SYNTHESIS

SYNOPSIS DESIGN VISION

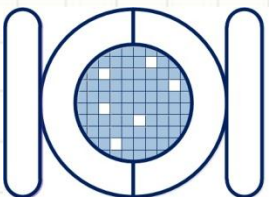


Digital Design Flow



Front-end

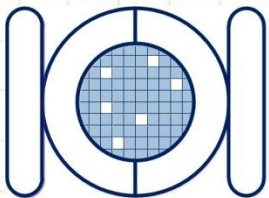
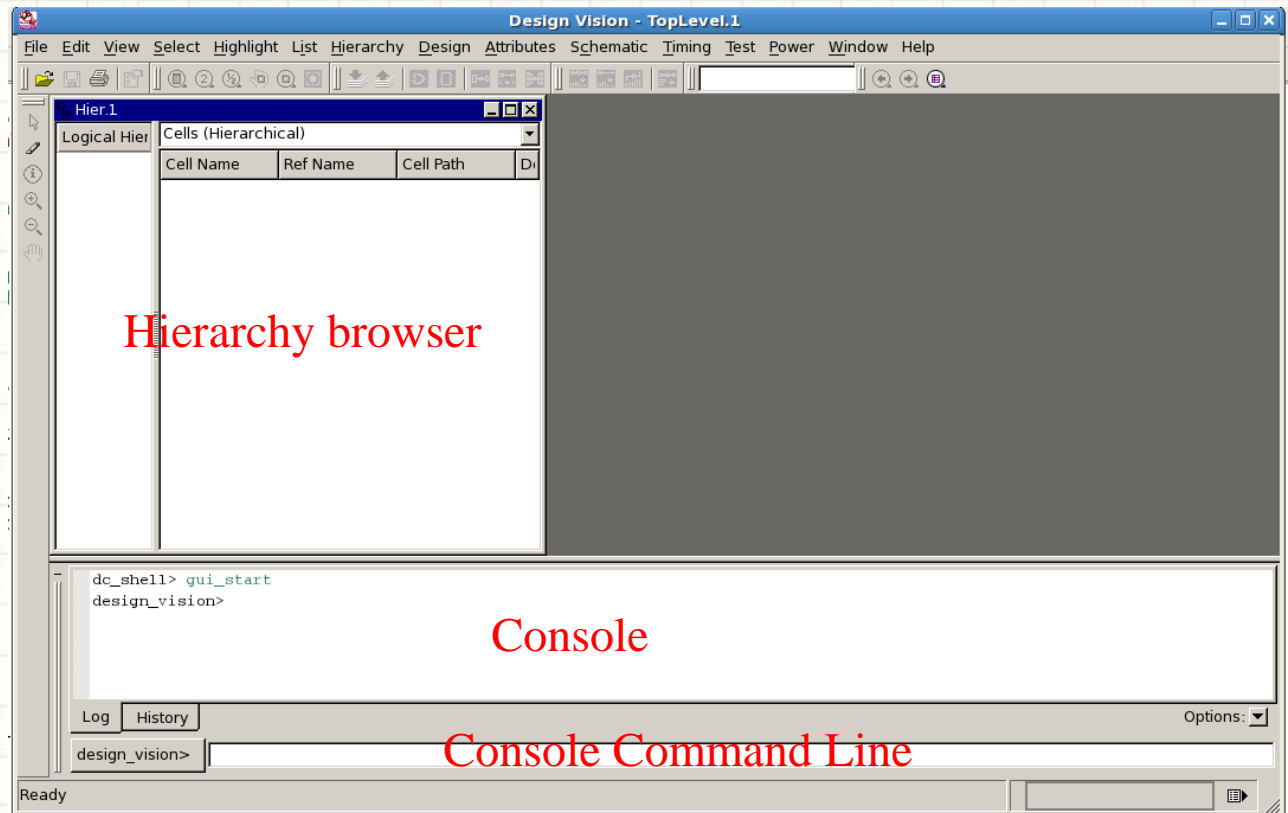
Back-end



Starting Design Vision

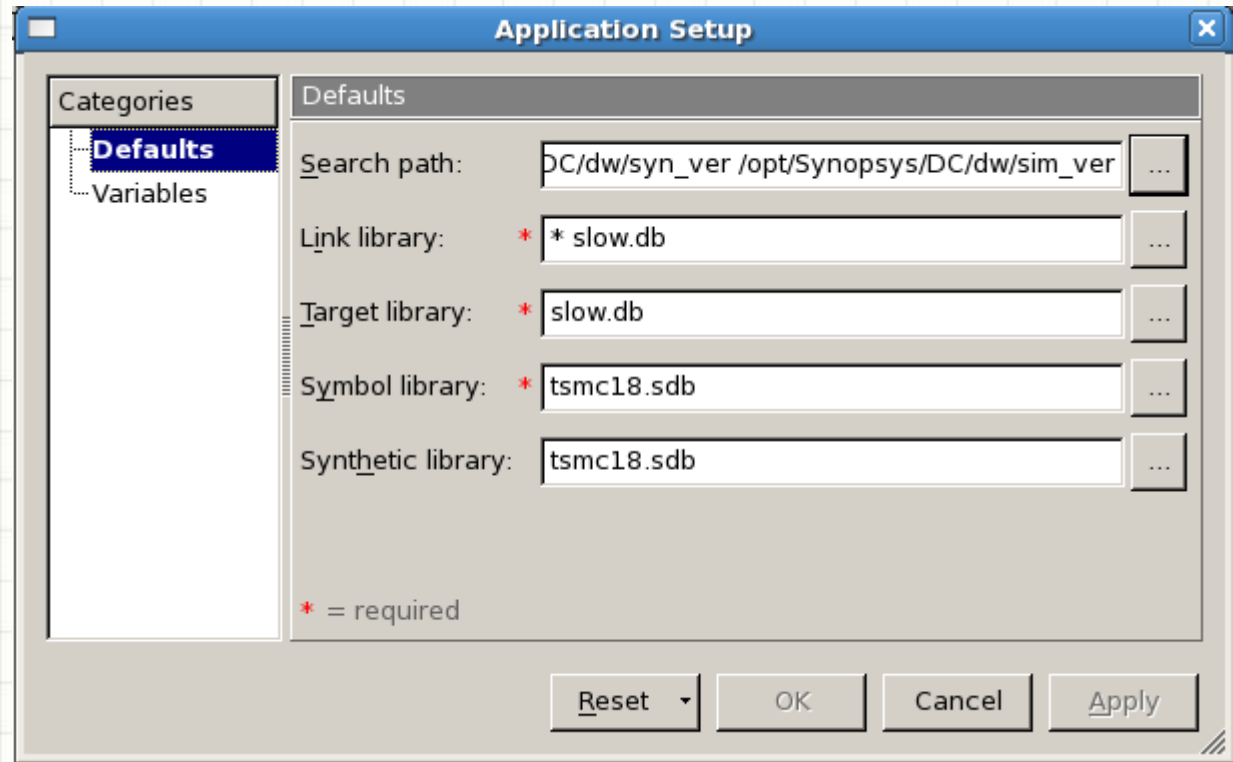
```
[user#@ICICHP home]$ cd digital_workshop/synthesis
```

```
[user#@ICICHP synthesis]$ design_vision
```

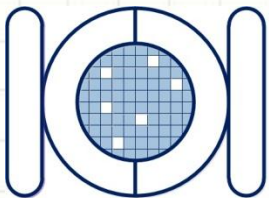


Setup

File -> Setup

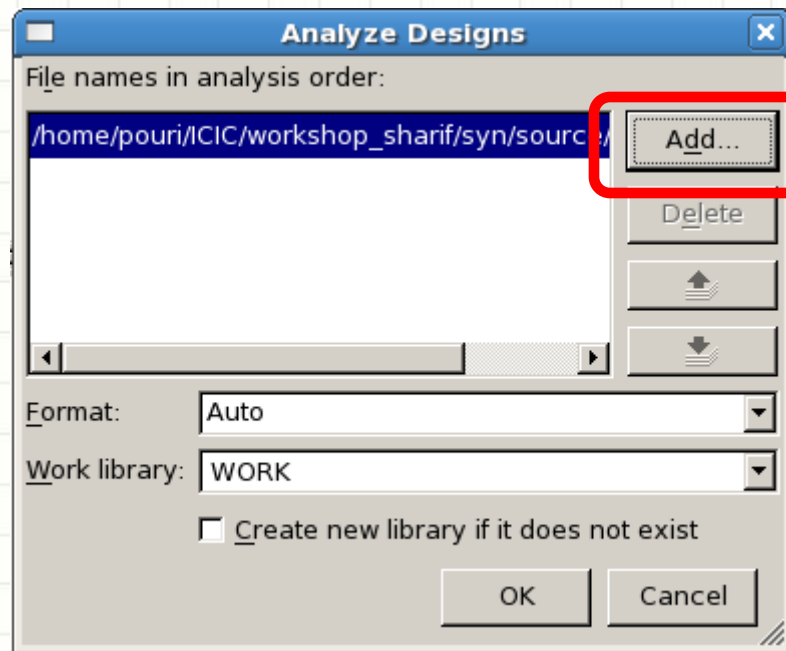


/home/pouri/digital_workshop/synthesis/.synopsys_dc.setup

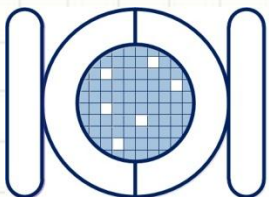


RTL HDL Model Analysis

File -> Analyze

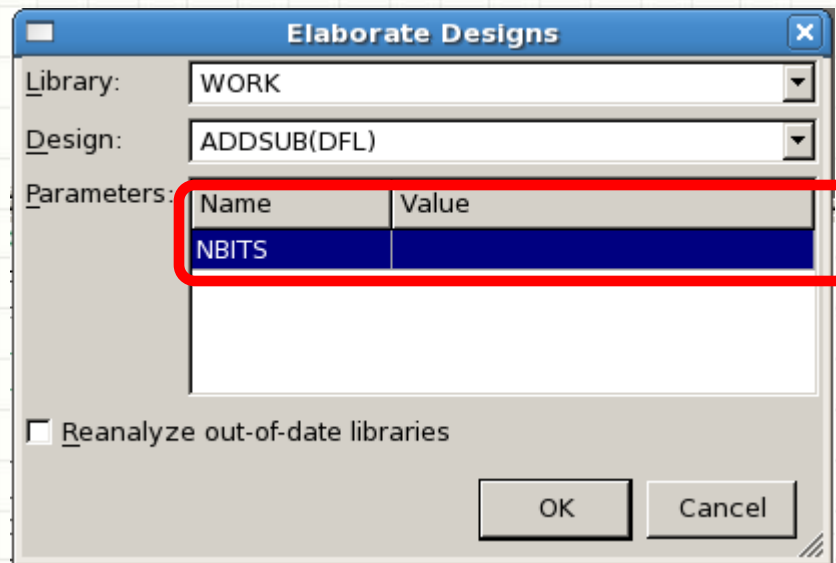


```
analyze -library WORK -format vhdl
```

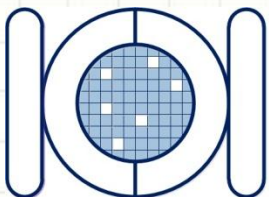


Design elaboration

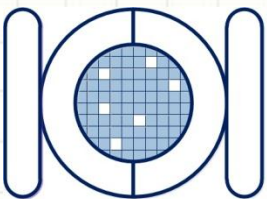
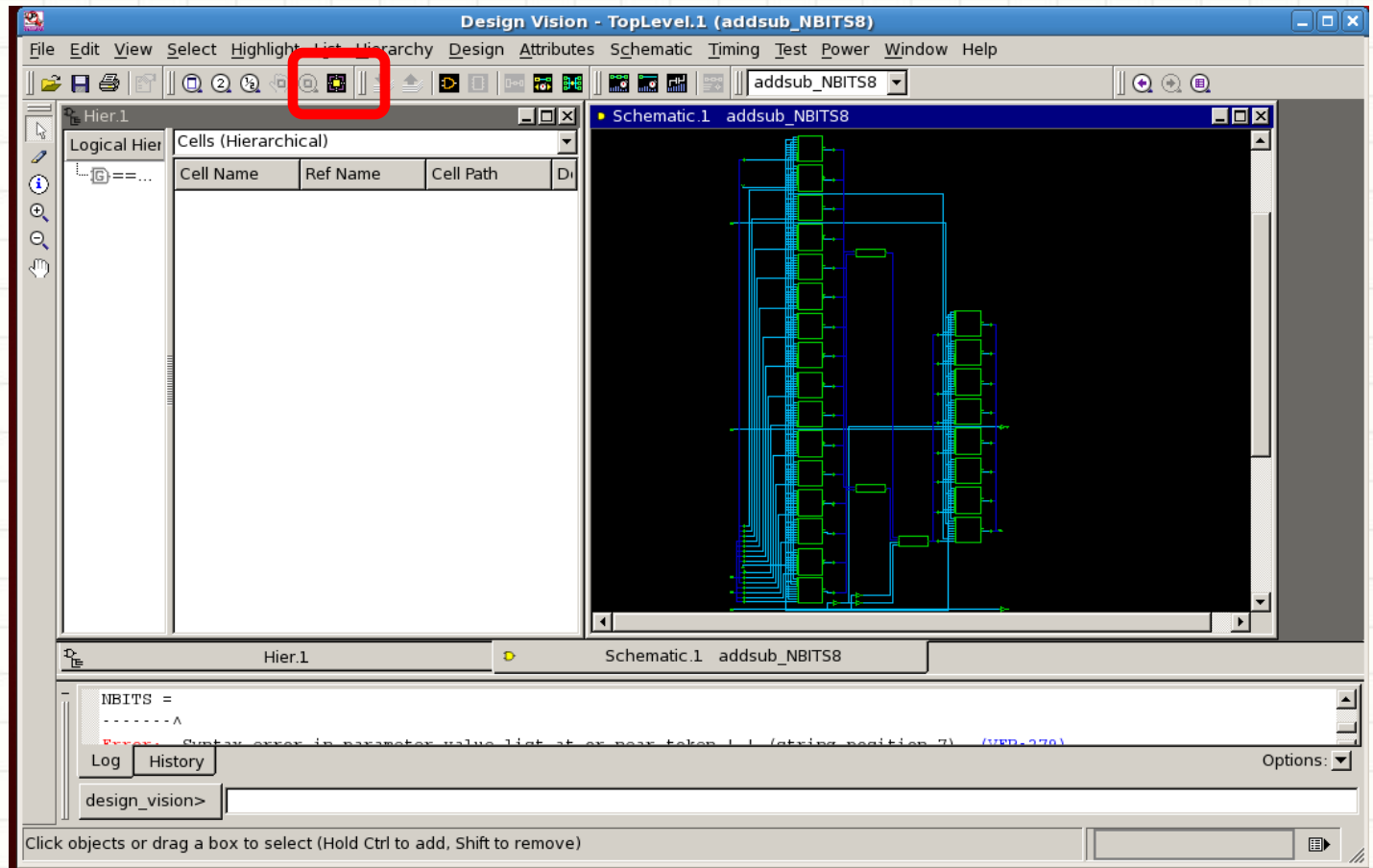
File -> Elaborate



```
elaborate ADDSUB -architecture DFL -library WORK -parameters  
"NBITS = 8"
```

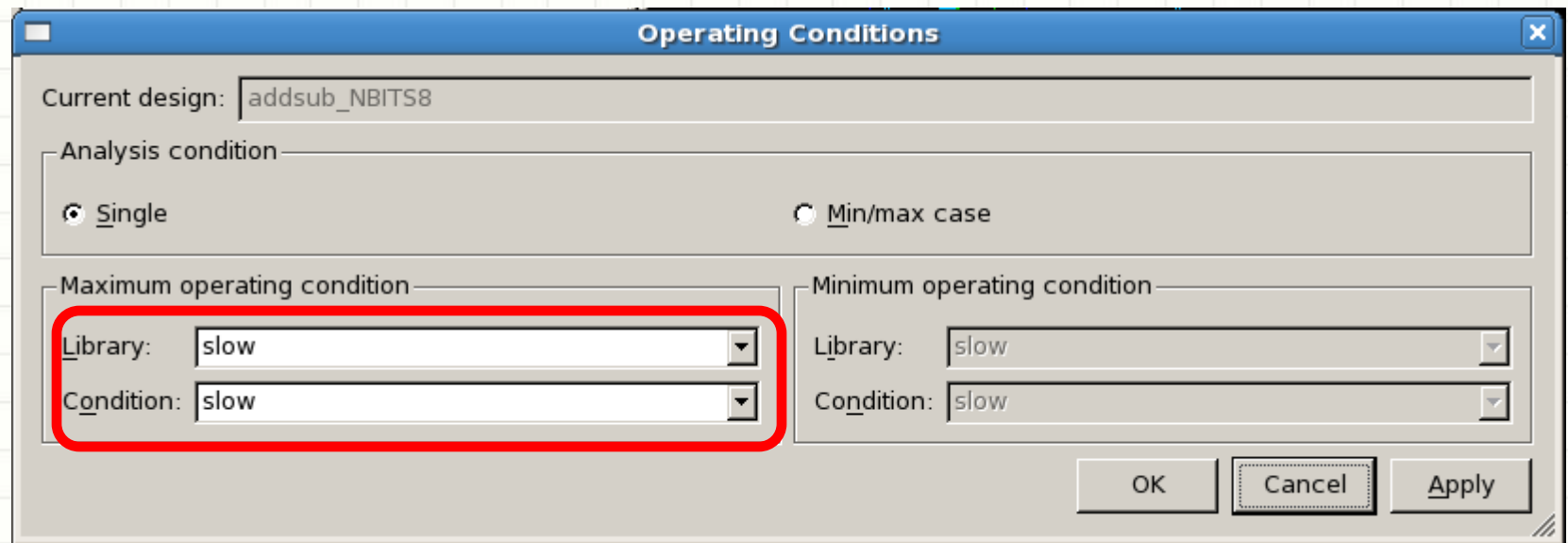


Create design Schematic

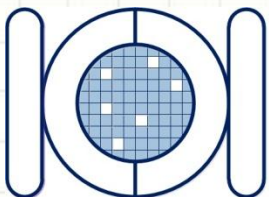


Design Environment Definition

Attributes -> Operating Environment -> operating Condition

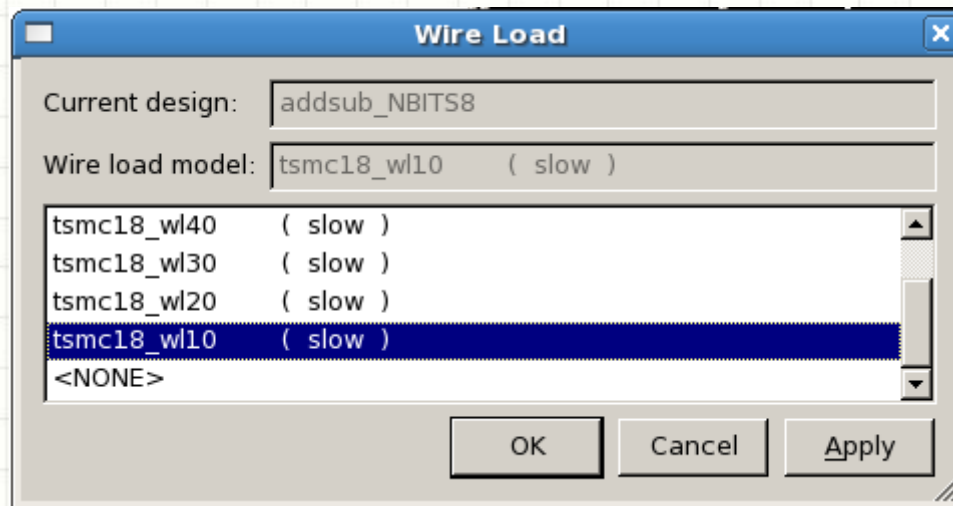


```
set_operating_conditions -library slow slow
```

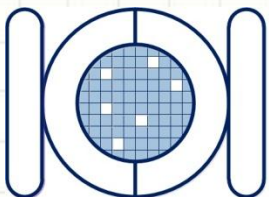


Design Environment Definition

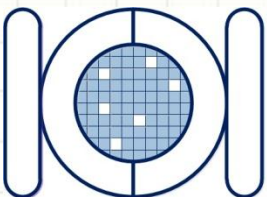
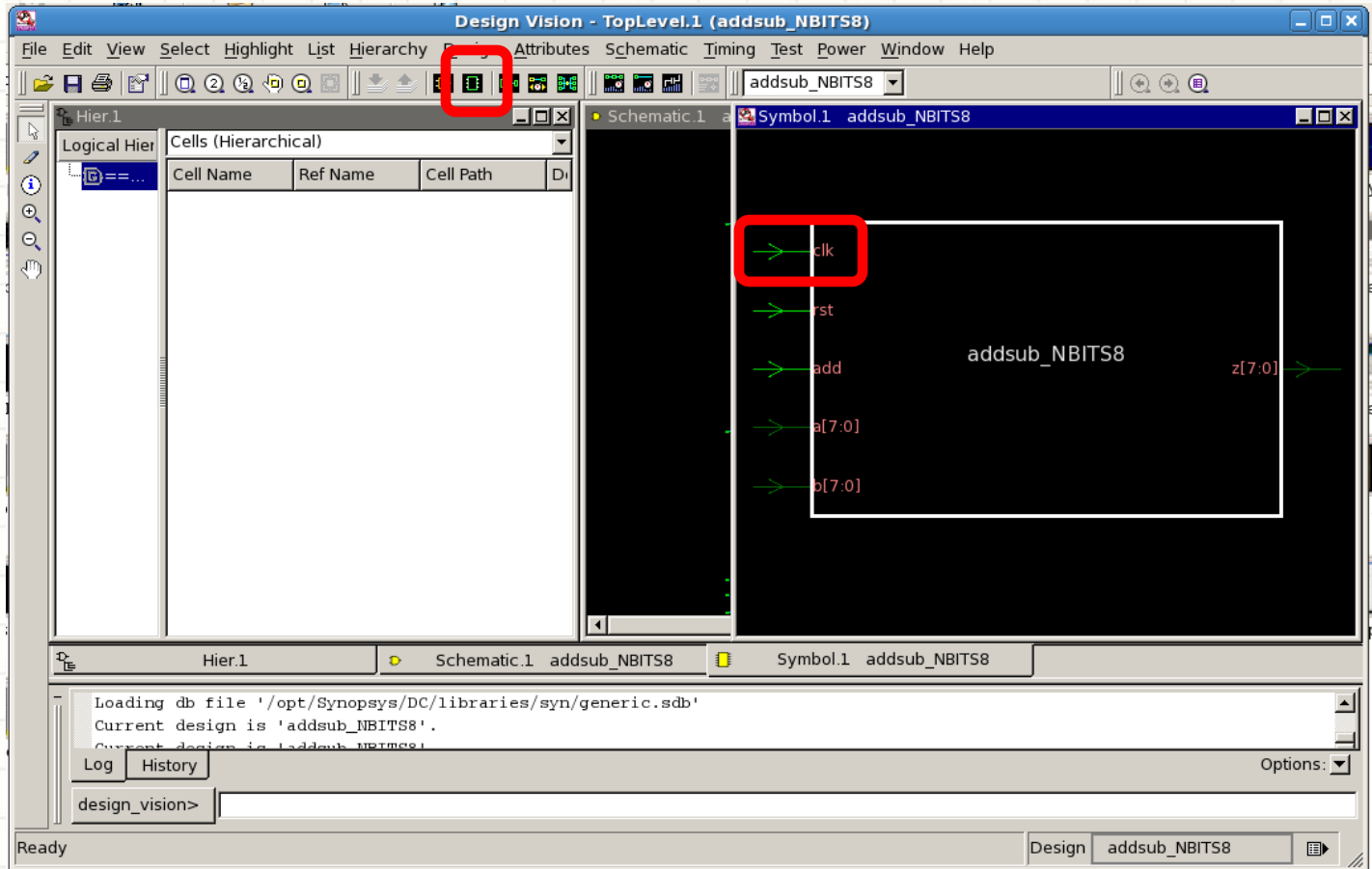
Attributes -> Operating Environment -> Wire Load



```
set_wire_load_model -name tsmc18_wl10 -library slow
```



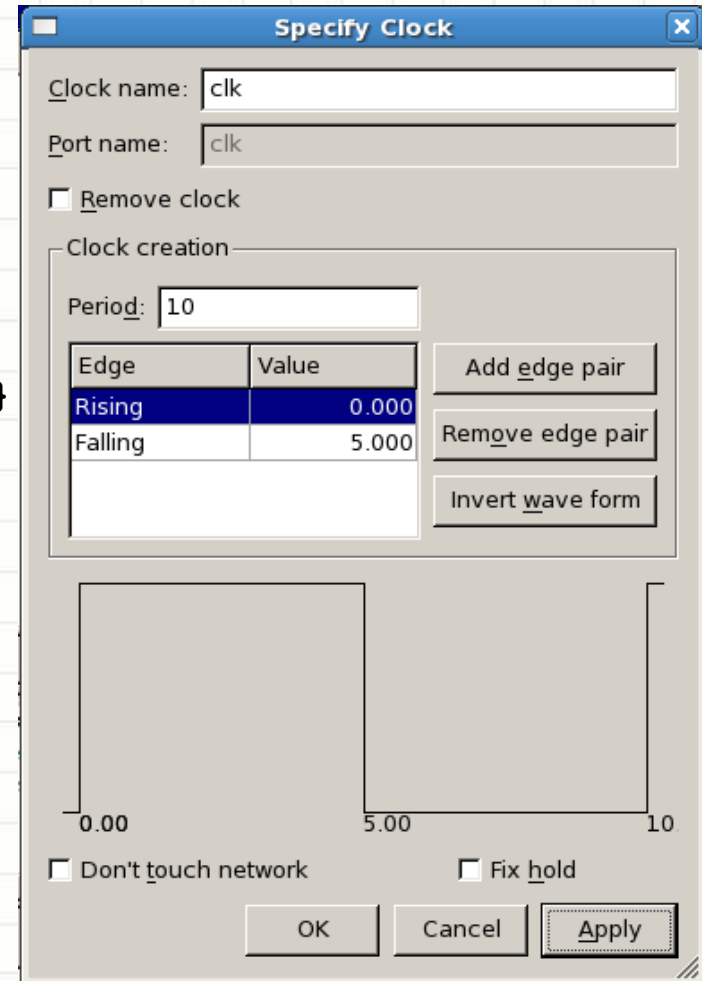
Design Constraint Definition



Design Constraint Definition

Attributes -> Specify Clock...

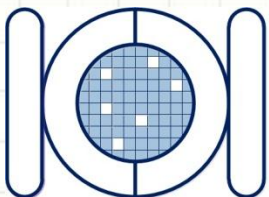
```
create_clock -name "clk"  
-period 10 -waveform {0 5}{ clk }
```



The 'Specify Clock' dialog box is shown with the following settings:

- Clock name: clk
- Port name: clk
- Remove clock
- Clock creation:
 - Period: 10
 - Edge table:

Edge	Value
Rising	0.000
Falling	5.000
 -
 -
 -
- Don't touch network
- Fix hold
- Buttons: OK, Cancel, Apply



Design Constraint Definition

Attributes -> Optimization Constraints -> Design Constraints...

```
set_max_area 0
```

Design Constraints

Current design:

Optimization constraints

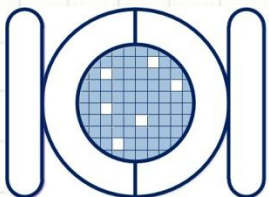
	Constraint value:	Unit:
Max <u>a</u> rea :	<input type="text" value="0"/>	
Max <u>d</u> ynamic power:	<input type="text"/>	<input type="checkbox"/>
Max <u>l</u> eakage power:	<input type="text"/>	<input type="checkbox"/>
Max <u>t</u> otal power:	<input type="text"/>	<input type="checkbox"/>

Design rules

Max fanout:

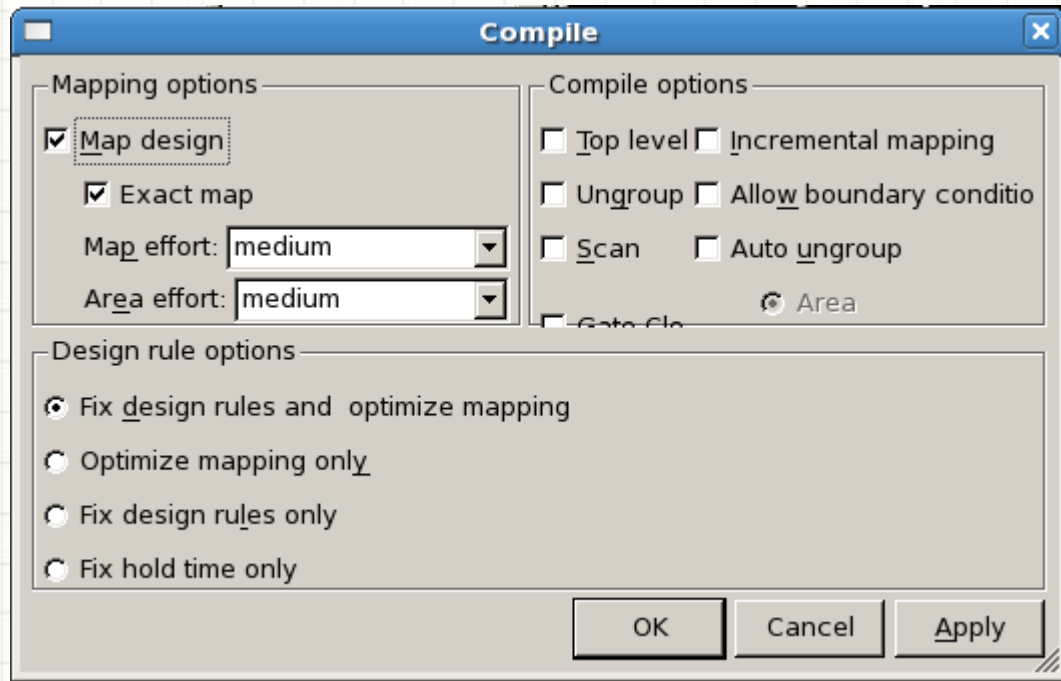
Max transition:

OK Cancel Apply

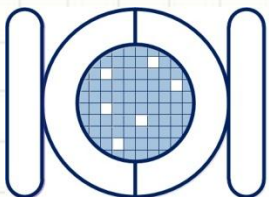


Design Mapping and Optimization

Design -> Compile Ultra...



```
compile_ultra -map_effort medium -area_effort medium
```



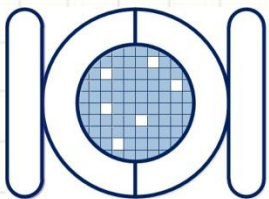
Report Generation and Outputs

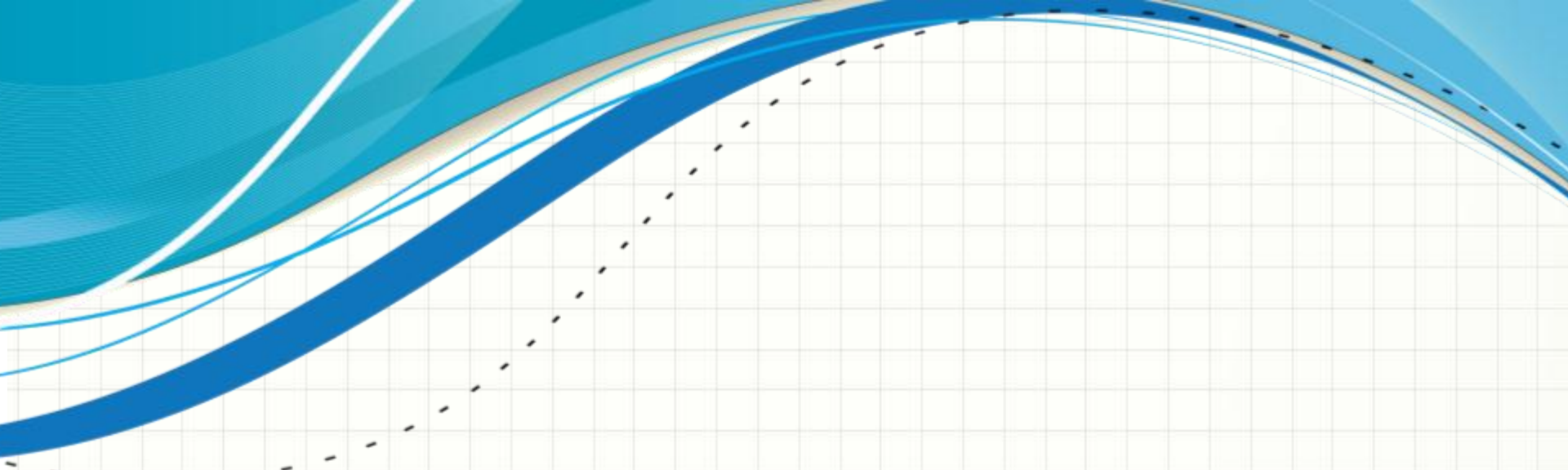
Design -> Report Area...

Timing -> Report Timing Path

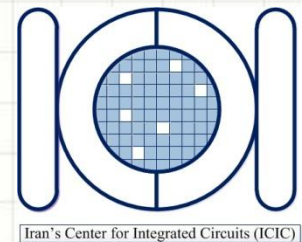
```
write -hierarchy -format ddc -output ./out/addsub.ddc
```

```
write -hierarchy -format verilog -output ./out/addsub.v
```





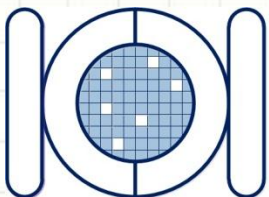
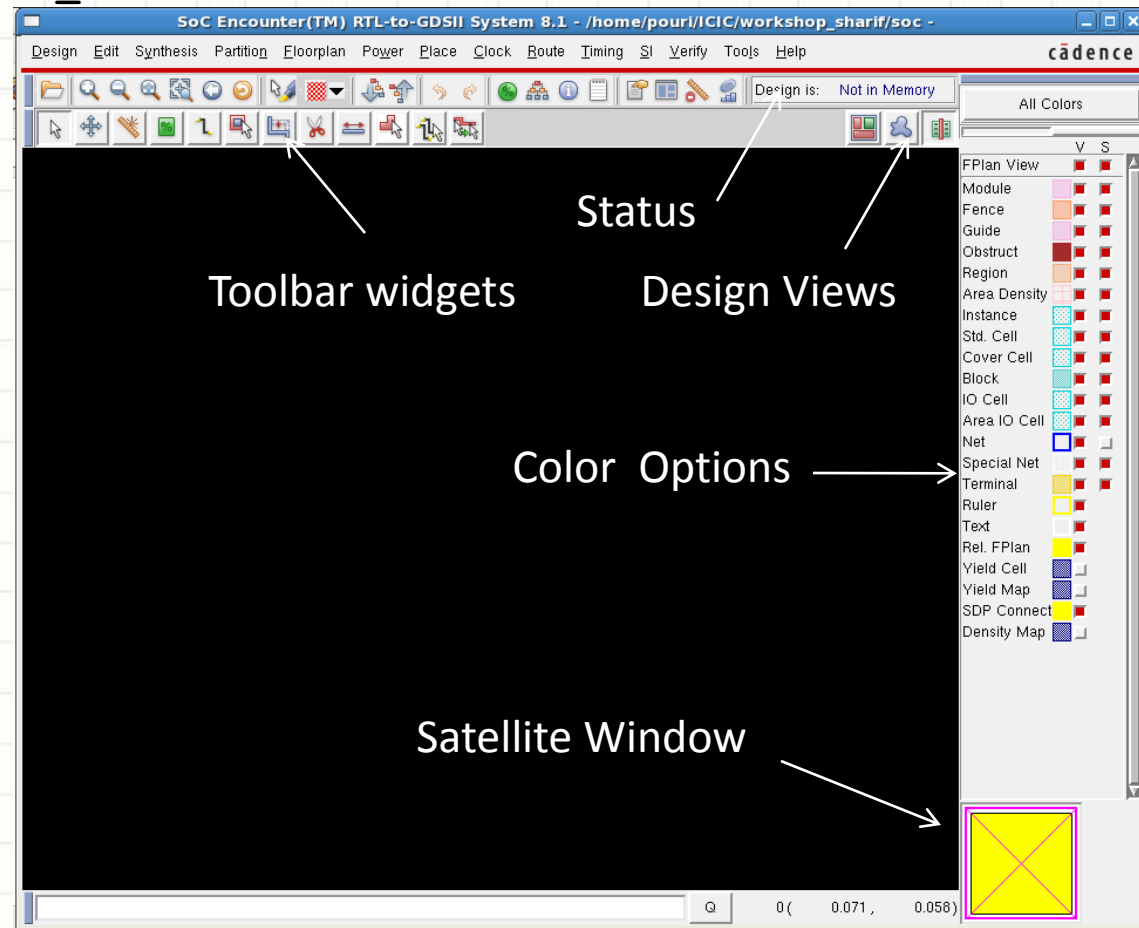
STANDARD CELL PLACEMENT AND ROUTING CADENCE SOC ENCOUNTER



Starting SOC Encounter

```
[user#@ICICHP home]$ cd digital_workshop/place_Route
```

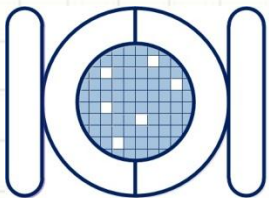
```
[user#@ICICHP place_Route]$ encounter
```



Setting

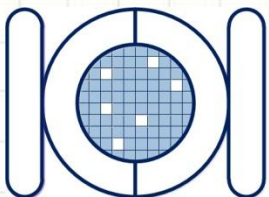
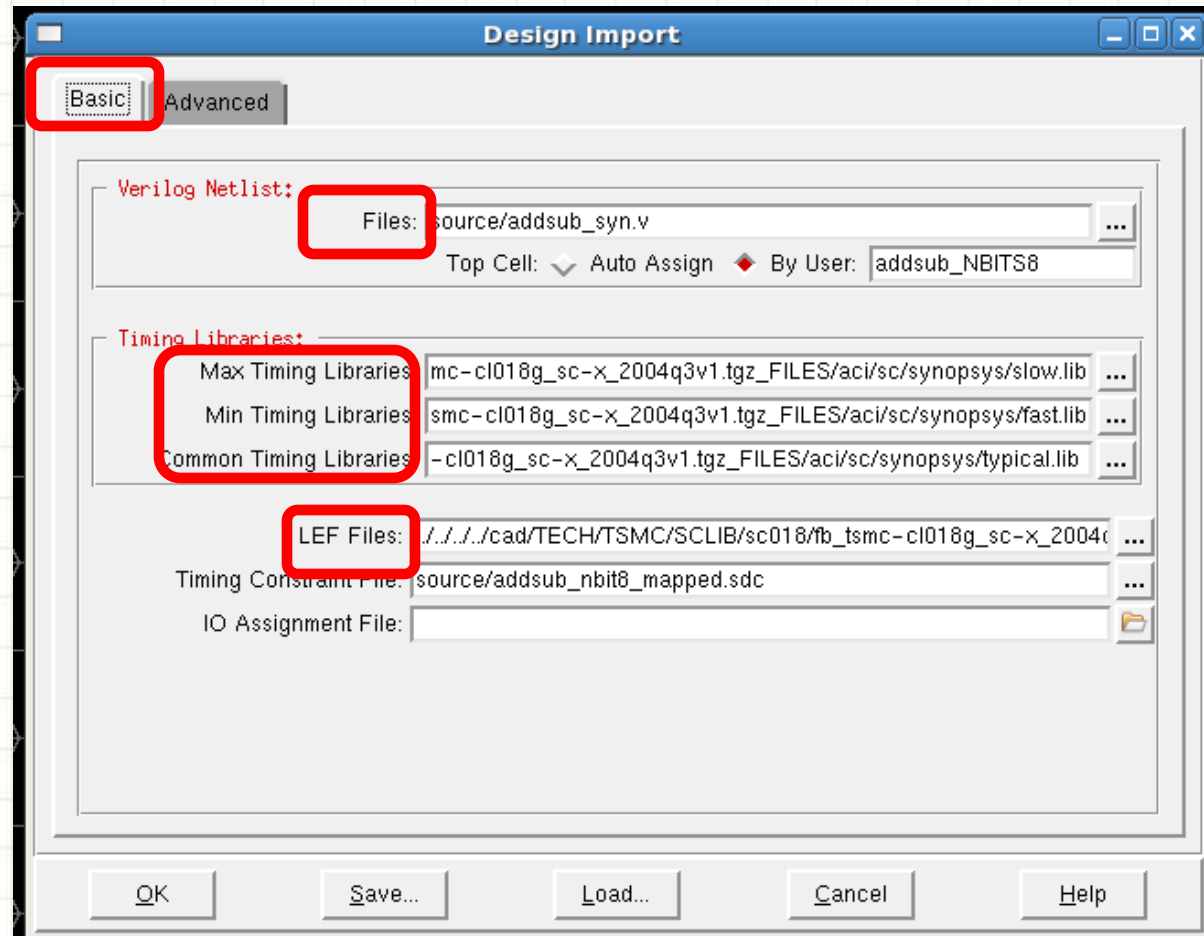
gedit source/addsub_NBITS8.conf

```
#####  
# #  
# FirstEncounter Input configuration file #  
# #  
#####  
# Created by First Encounter v08.10-s338_1 on Sat Nov 12 12:31:56 2011  
global rda_Input  
set cwd /home/pouri/digital_workshop/place_Route  
set rda_Input(import_mode) { -treatUndefinedCellAsBbox 0 -  
keepEmptyModule 1 -useLefDef56 1 }
```



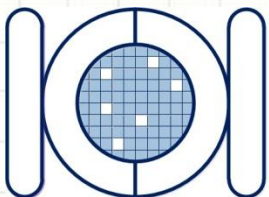
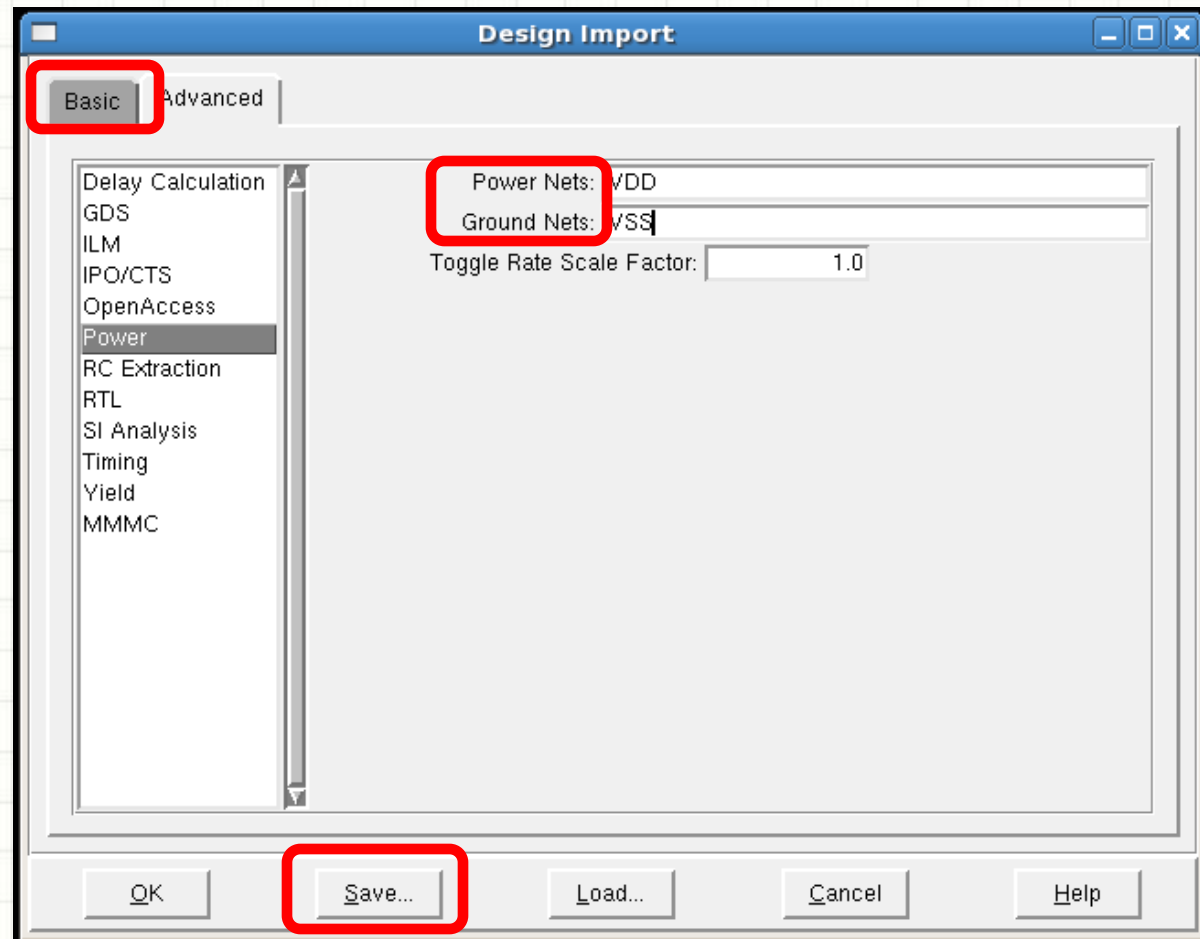
Design Import

Design -> Design Import

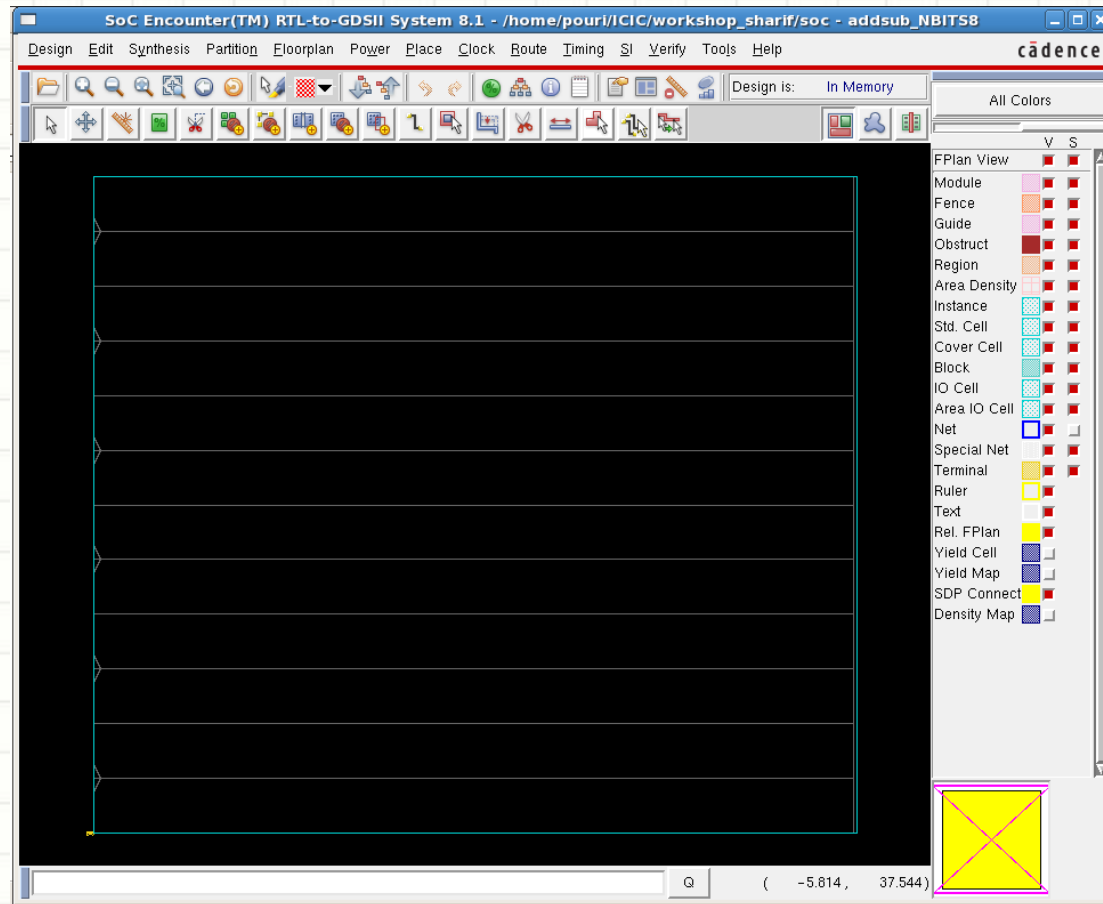


Design Import

Design -> Design Import

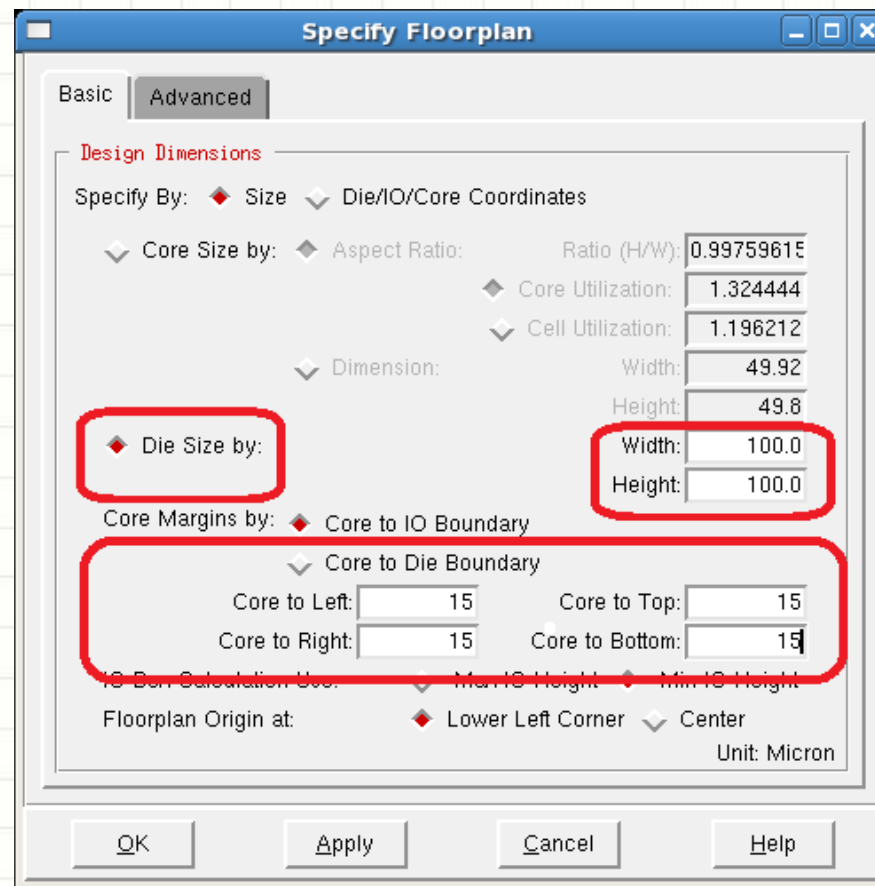


Design Import



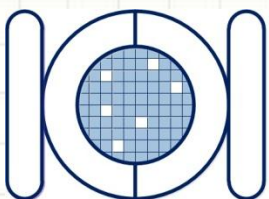
Floorplan Specification

Floorplan -> Specify Floorplan



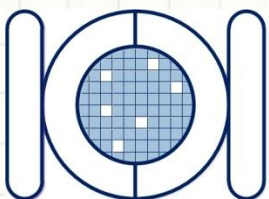
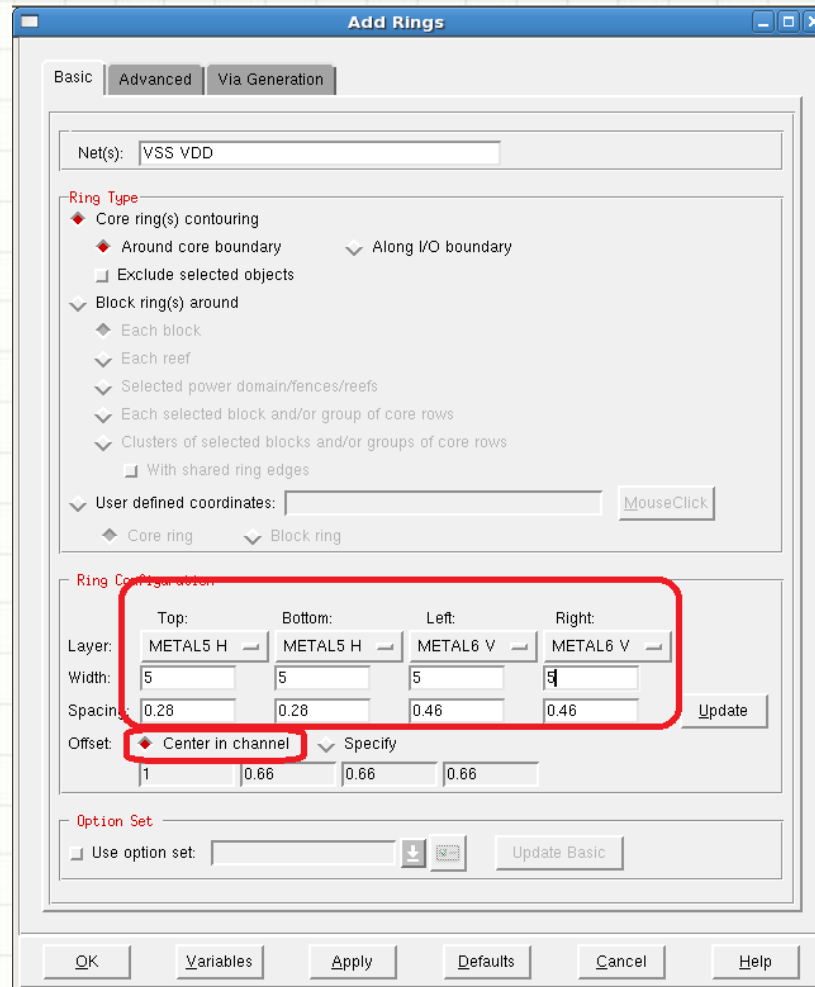
The image shows a 'Specify Floorplan' dialog box with the 'Advanced' tab selected. The 'Design Dimensions' section is expanded, showing 'Specify By' set to 'Size'. Under 'Core Size by', 'Die Size by' is selected and circled in red. The 'Dimension' section shows 'Width' and 'Height' both set to 100.0, also circled in red. The 'Core Margins by' section is set to 'Core to Die Boundary', and the 'Core to Die Boundary' section is circled in red, showing 'Core to Left', 'Core to Right', 'Core to Top', and 'Core to Bottom' all set to 15. The 'Floorplan Origin at' is set to 'Lower Left Corner'. The unit is 'Micron'.

Property	Value
Ratio (H/W)	0.99759615
Core Utilization	1.324444
Cell Utilization	1.196212
Width	49.92
Height	49.8
Die Size by: Width	100.0
Die Size by: Height	100.0
Core to Left	15
Core to Right	15
Core to Top	15
Core to Bottom	15

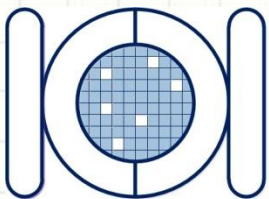
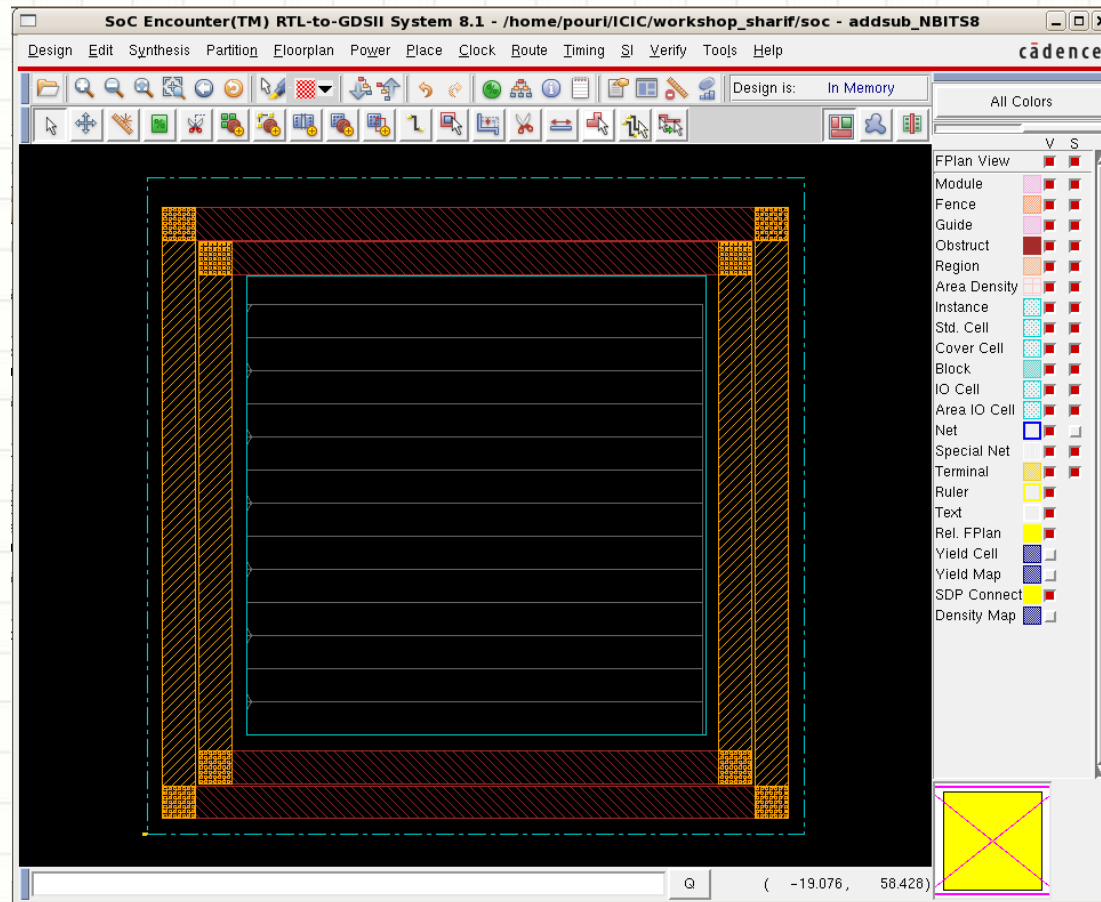


Power Planning- Add Rings

Power -> Power Planning -> Add Rings



Power Planning- Add Rings



Power Planning- Add Stripes

Power -> Power Planning -> Add Stripes

Basic | Advanced | Via Generation

Set Configuration

Net(s): VSS VDD

Layer: METAL5

Direction: vertical Horizontal

Width: 1

Spacing: 0.26 Update

Set Pattern

◆ Set-to-set distance: 100

Number of sets: 1

▽ Bumps ◆ Over ▾ Between

▽ Over P/G pins Pin layer: Top pin layer Max pin width: 0

◆ Master name: Selected blocks All blocks

Stripe Boundary

◆ Core ring

▽ Pad ring ▾ Inner ◆ Outer

▽ Design boundary Create pins

▽ Each selected block/domain/fence

▽ All domains

▽ Specify rectangular area

▽ Specify rectilinear area

Fixes / set Stripes

Start from: ▾ bottom ◆ top

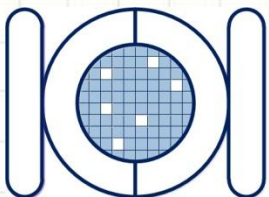
◆ Relative from core or selected area

Y from top: 30 Y from bottom: 0

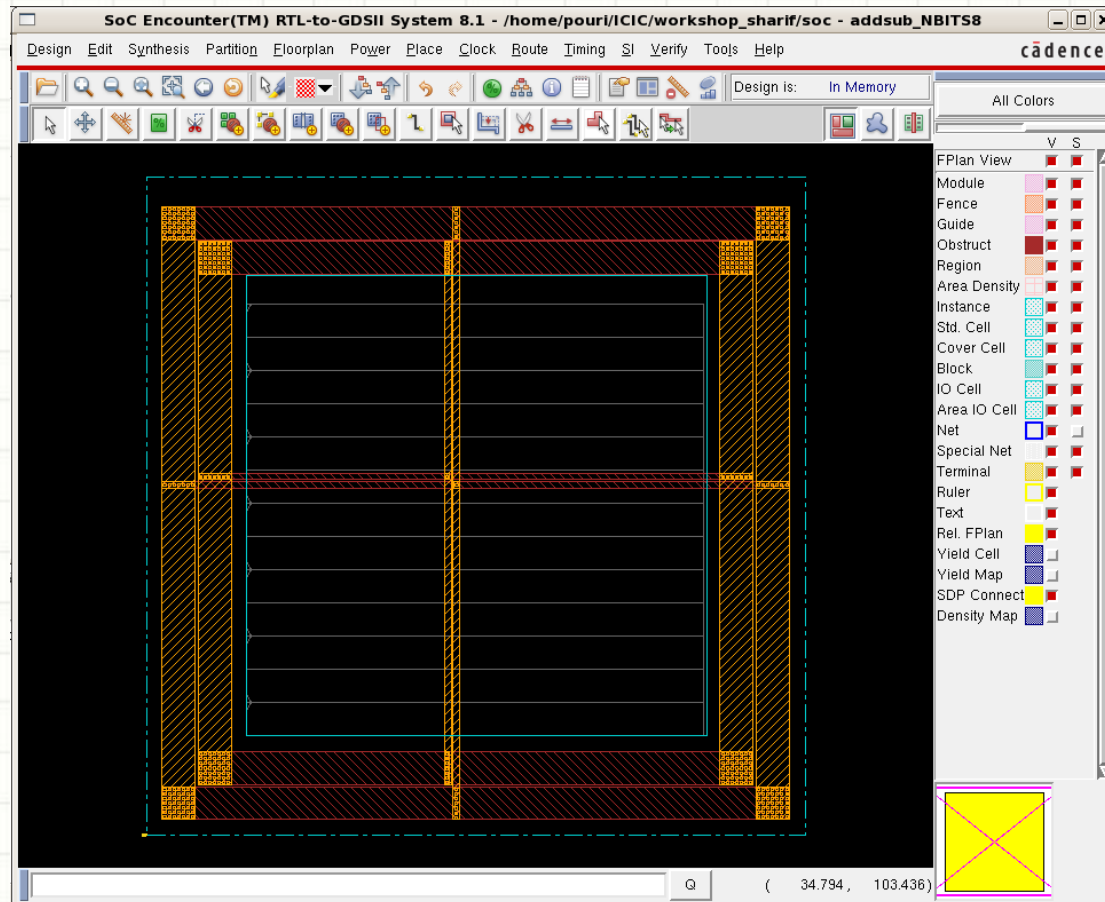
▽ Absolute locations

- Option Set

OK Variables Apply Defaults Cancel Help

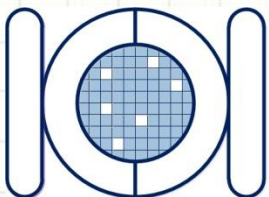
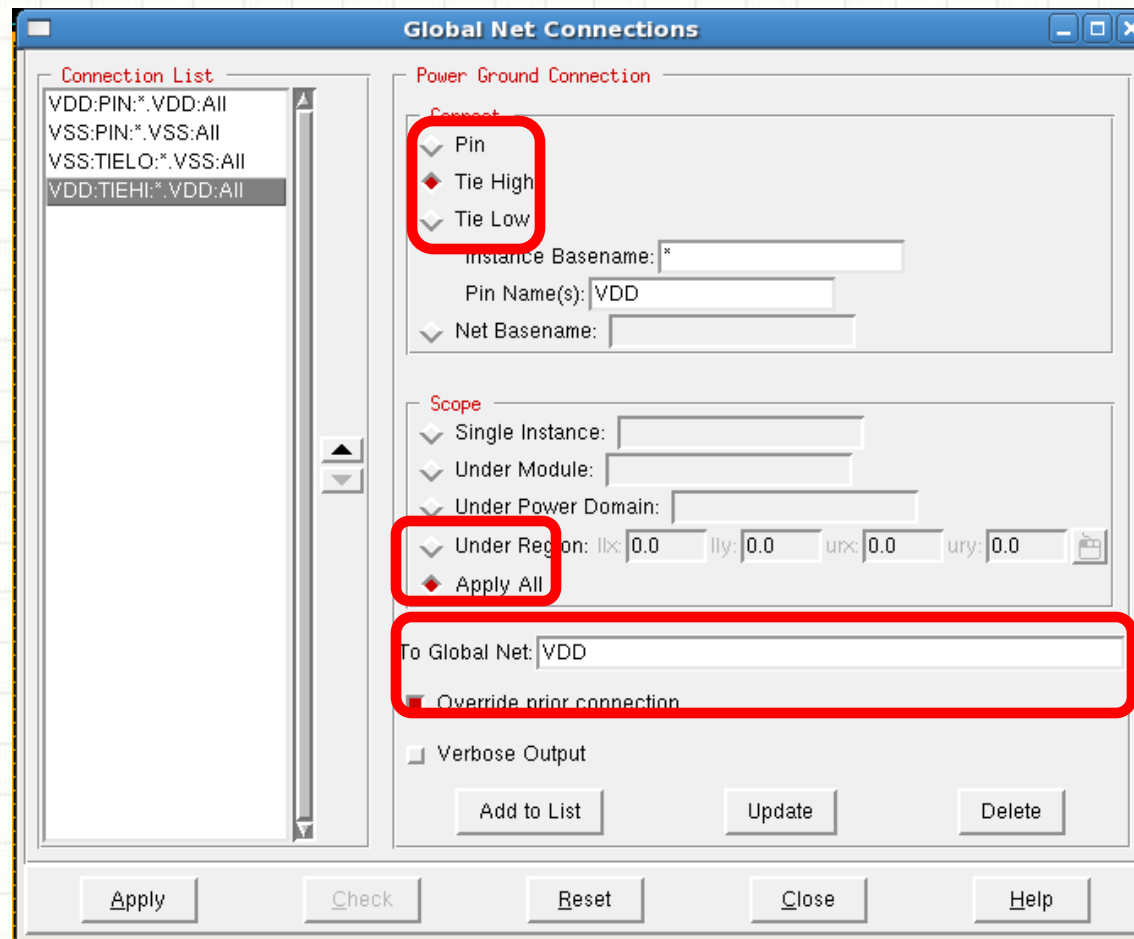


Power Planning- Add Stripes



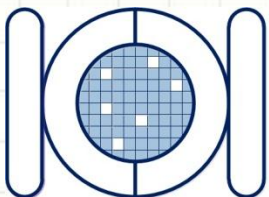
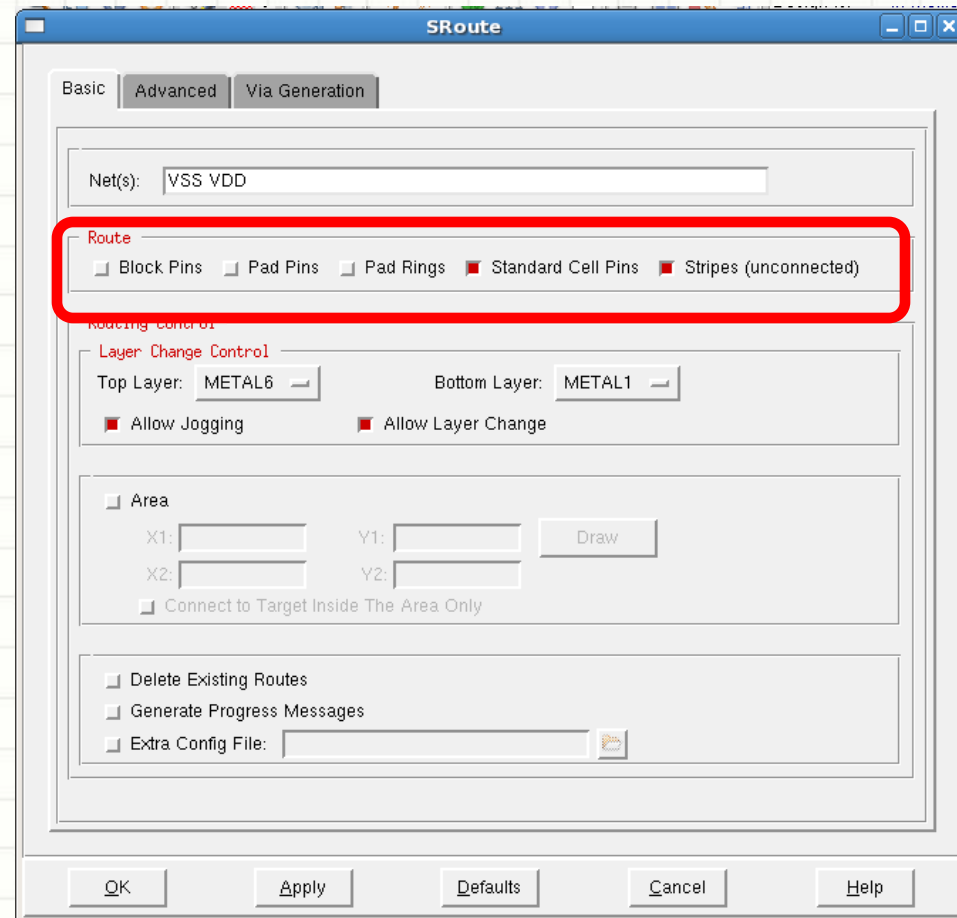
Global Net Connection

Floorplan -> Connect Global Nets

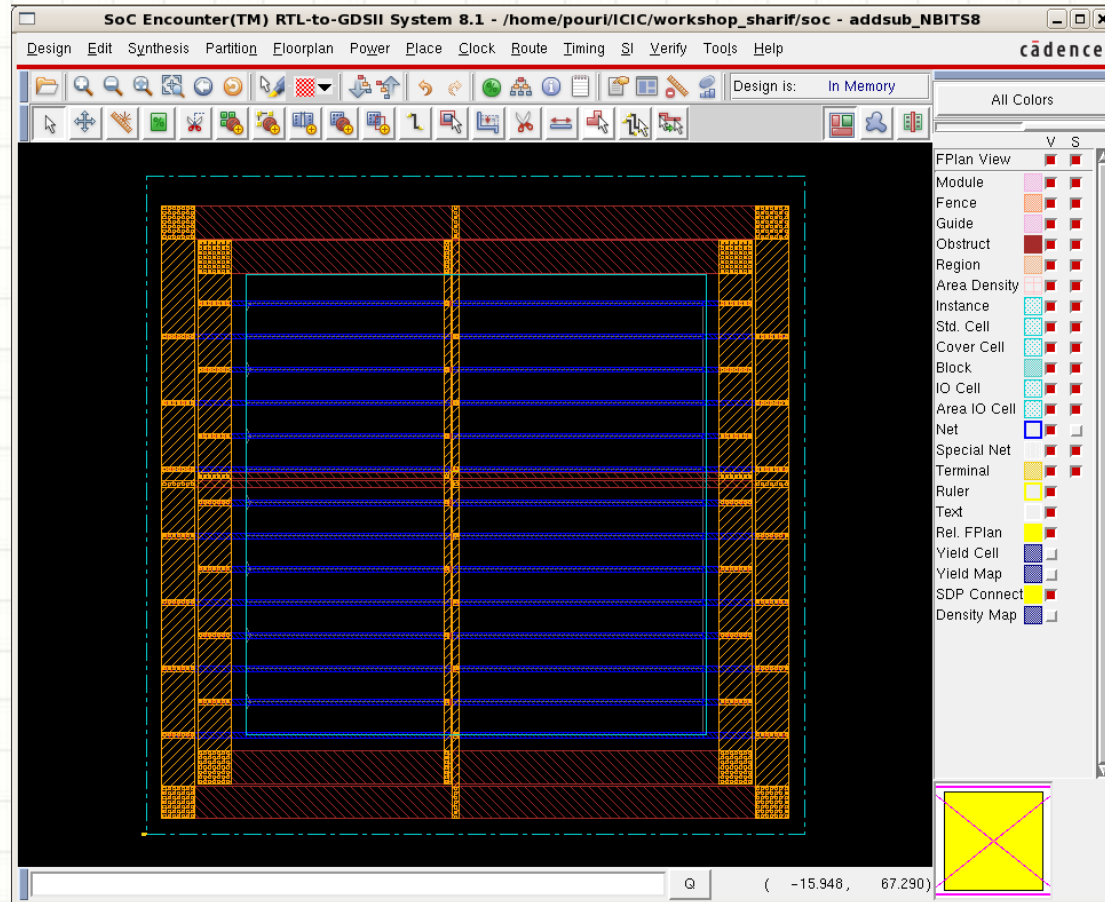


Sroute

Route -> Special Route...

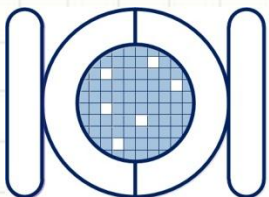
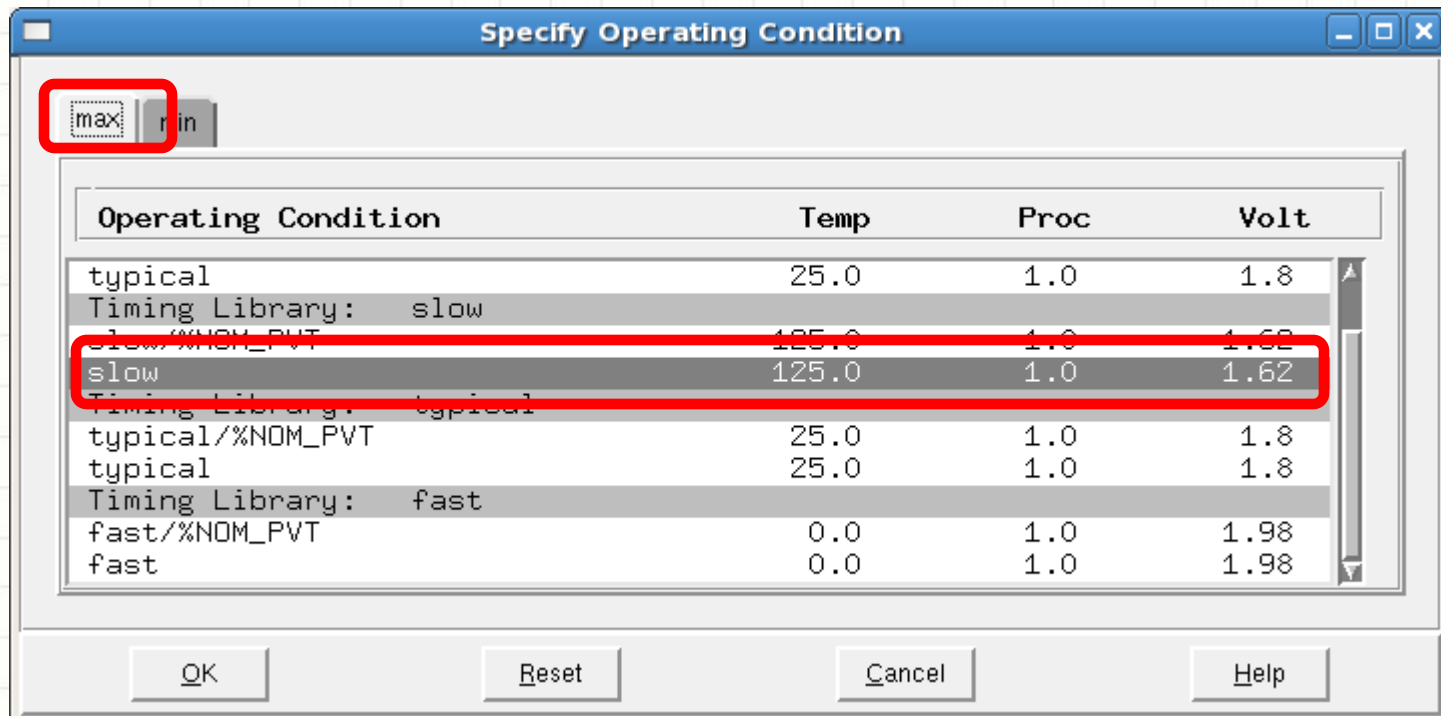


Sroute



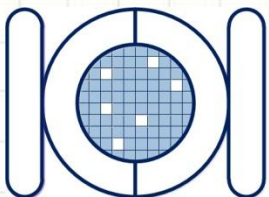
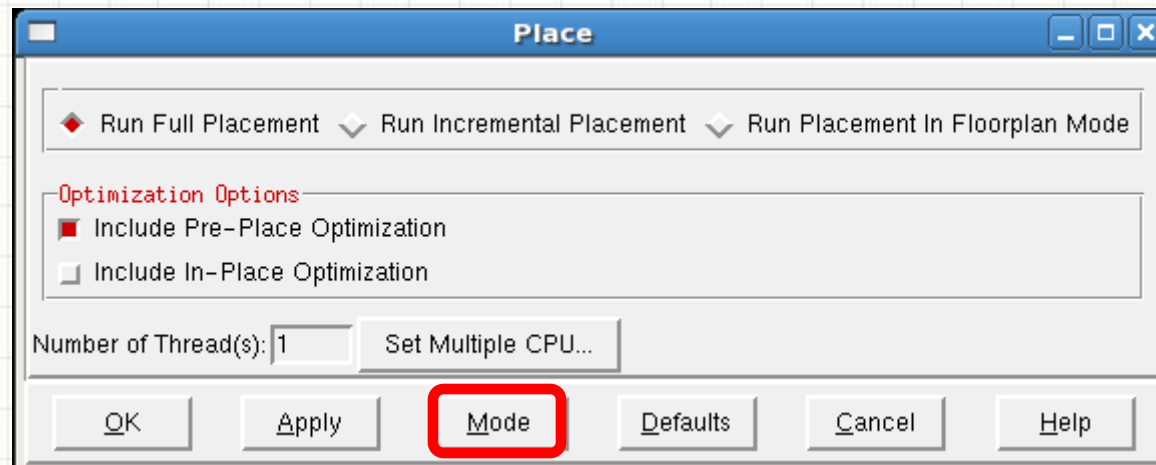
Operating Conditions Definition

Timing -> Analysis Condition -> Specify Operating Condition/PVT...



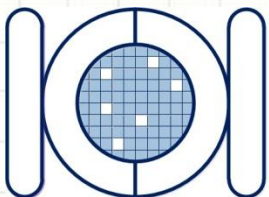
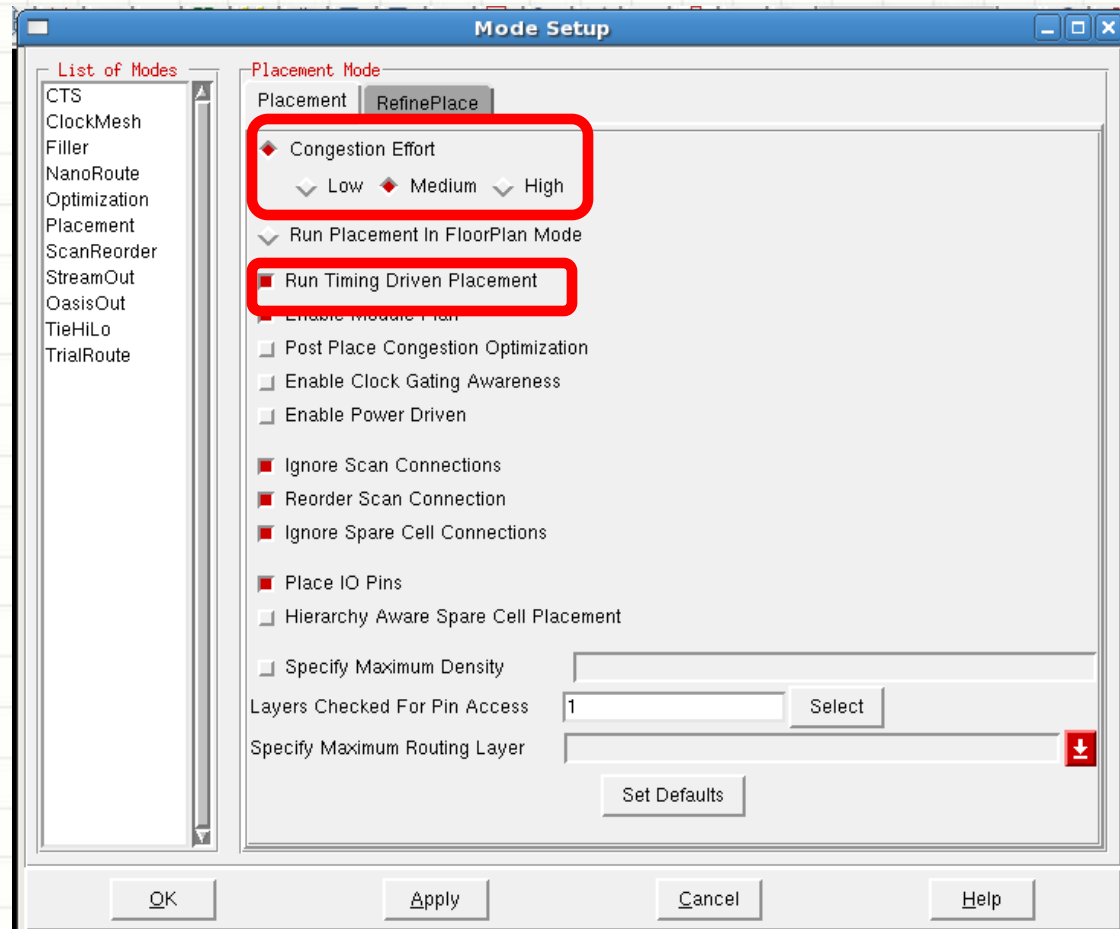
Core Cell Placement

Place -> Standard Cells...



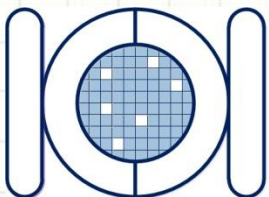
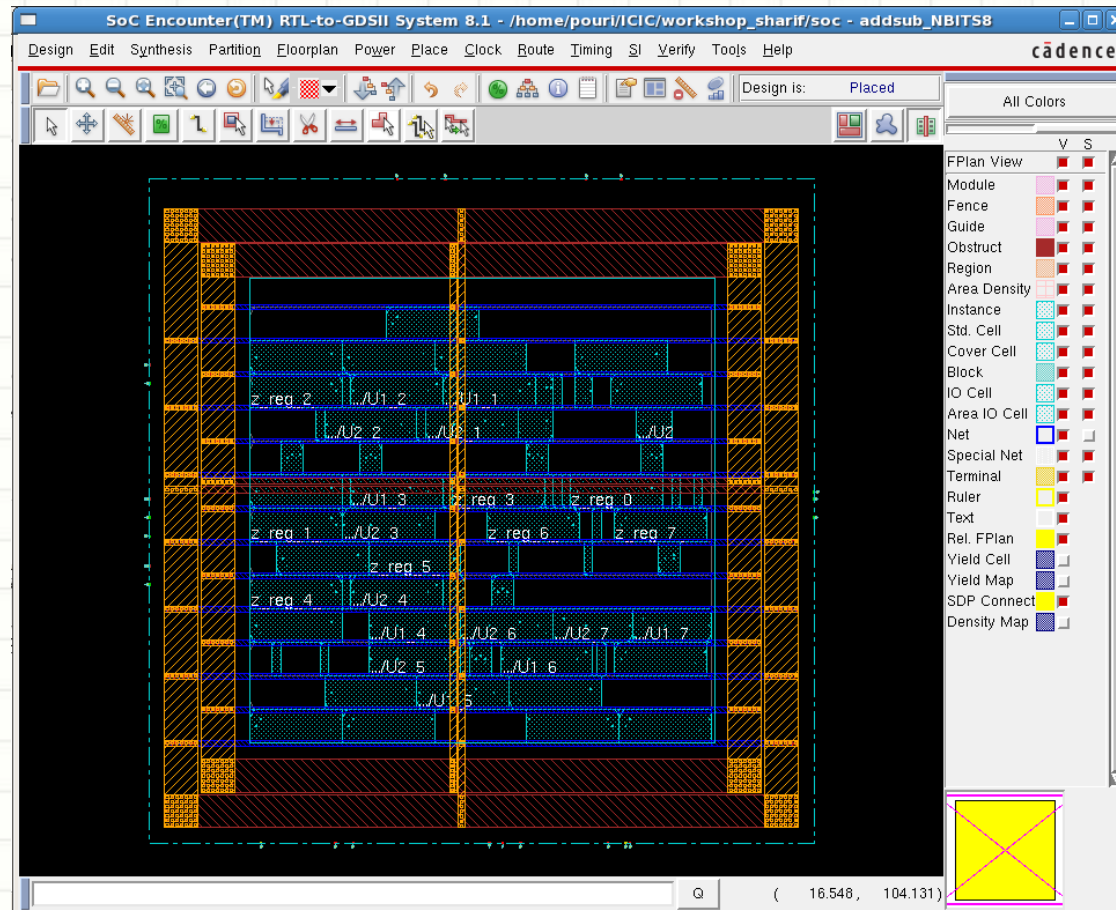
Core Cell Placement

Place -> Standard Cells...-> Mode



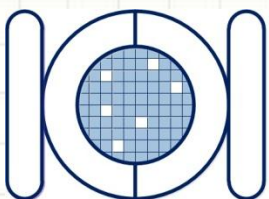
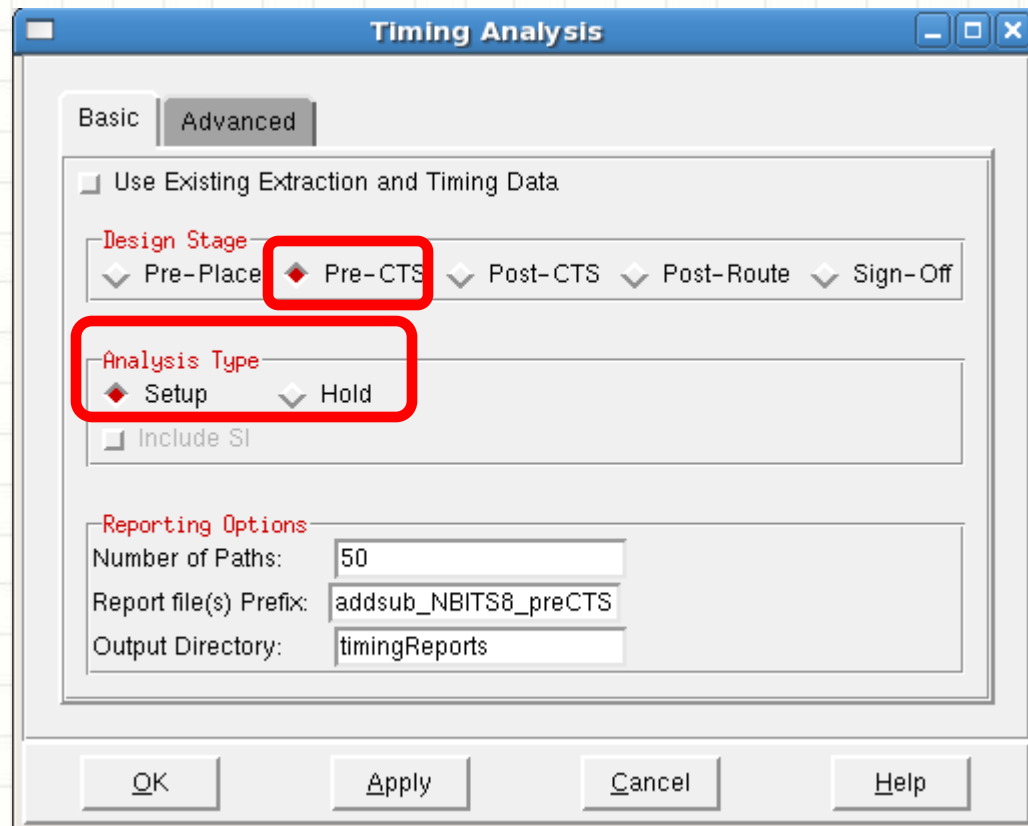
Core Cell Placement

Design -> Save Design As ... -> SoCE



Post-Placement Timing Analysis

Timing -> Analyze Timing...

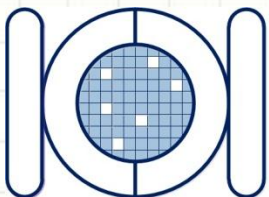


Post-Placement Timing Analysis

timeDesign Summary

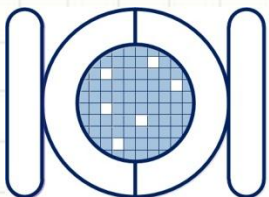
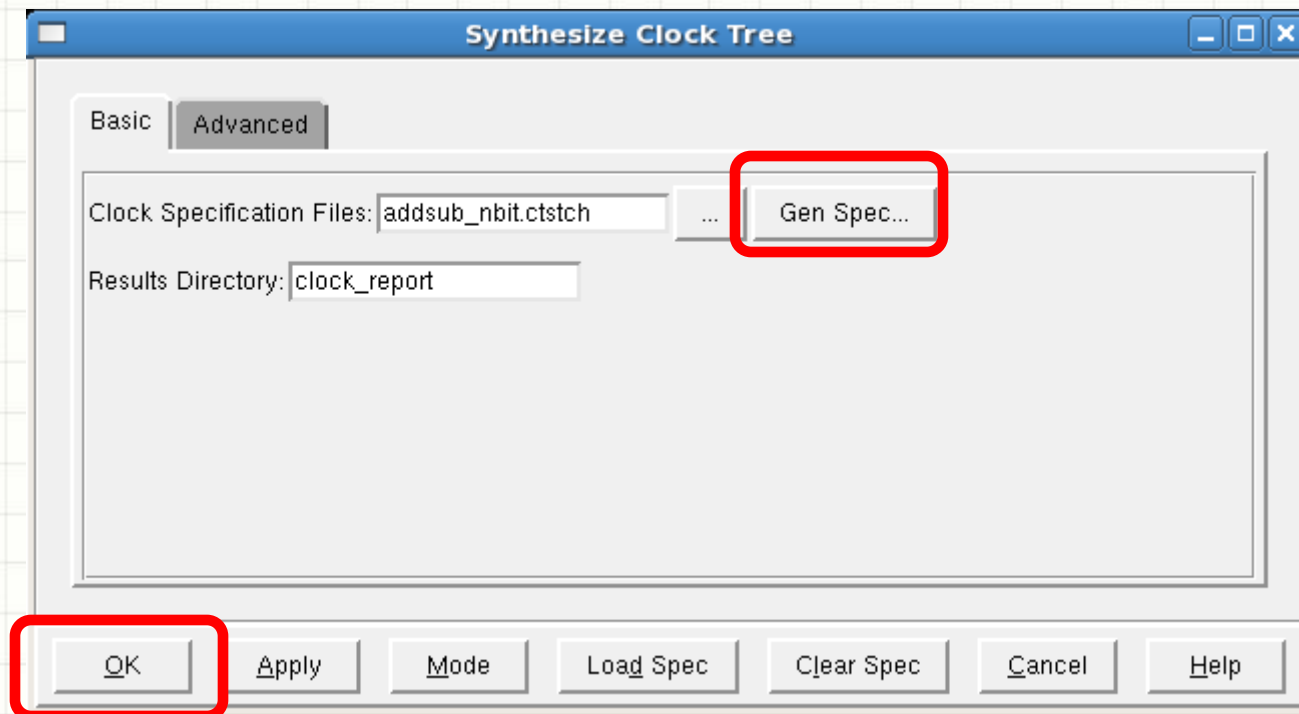
Setup mode	all	reg2reg	in2reg	reg2out	in2out	clkgate
WNS (ns):	6.042	6.042	9.034	N/A	N/A	N/A
TNS (ns):	0.000	0.000	0.000	N/A	N/A	N/A
Violating Paths:	0	0	0	N/A	N/A	N/A
All Paths:	48	8	48	N/A	N/A	N/A

DRVs	Real		Total
	Nr nets(terms)	Worst Vio	Nr nets(terms)
max_cap	0 (0)	0.000	0 (0)
max_tran	0 (0)	0.000	0 (0)
max_fanout	0 (0)	0	0 (0)

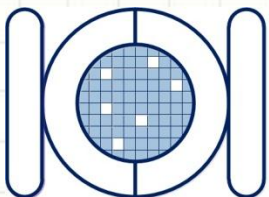
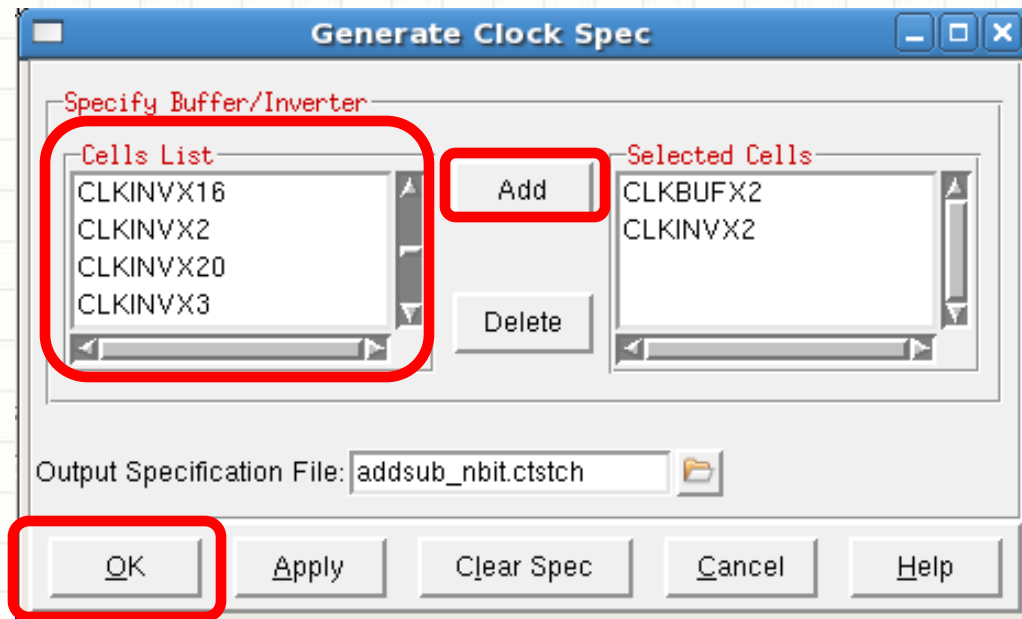


Clock Tree Synthesis

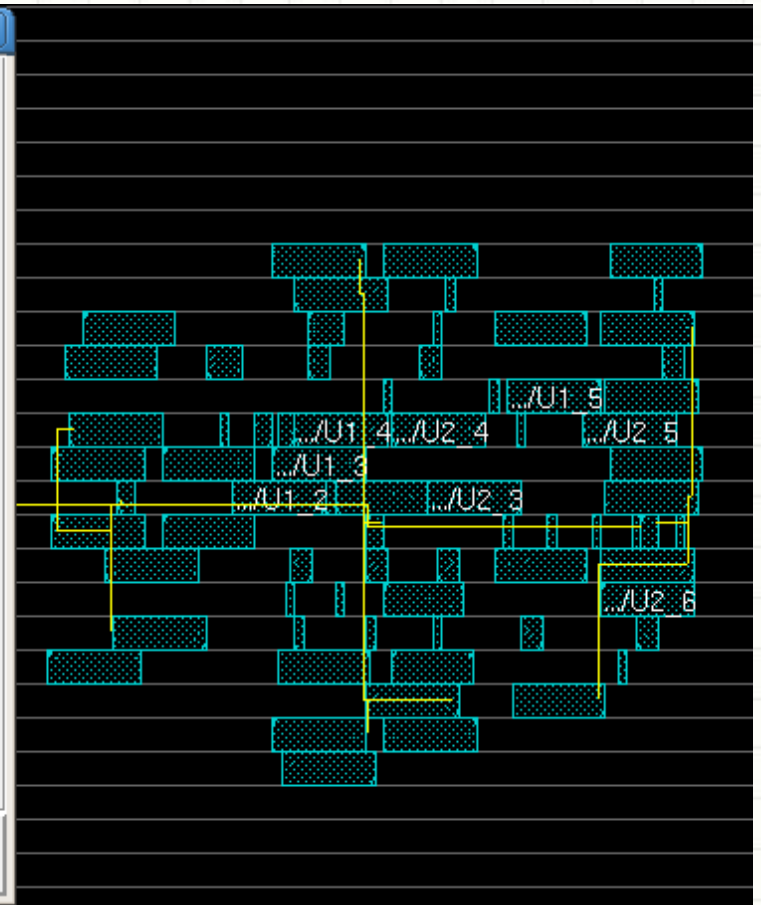
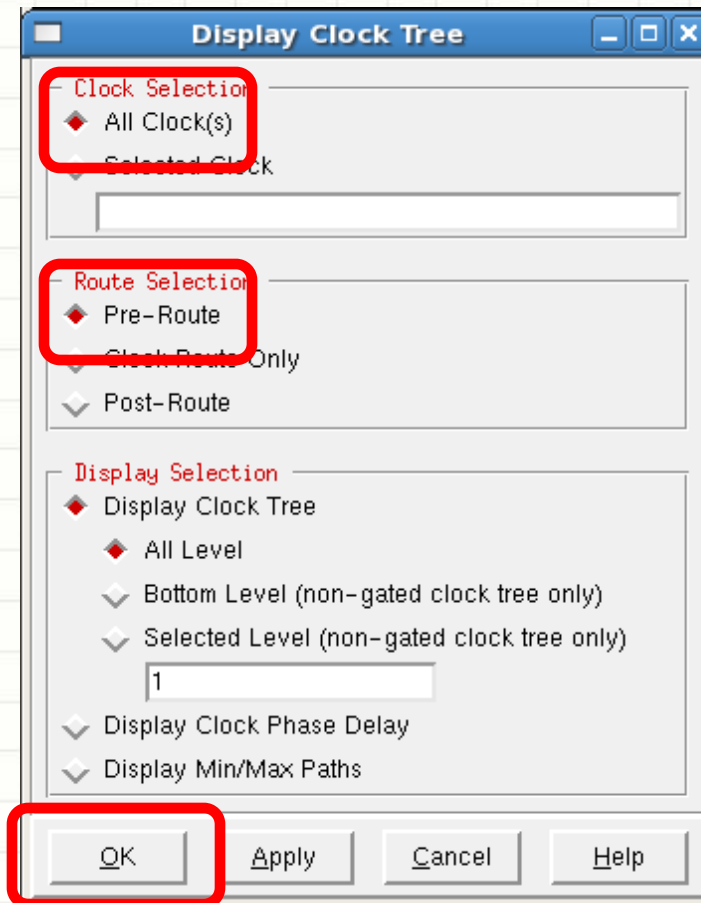
Clock -> Design Clock...



Clock Tree Synthesis

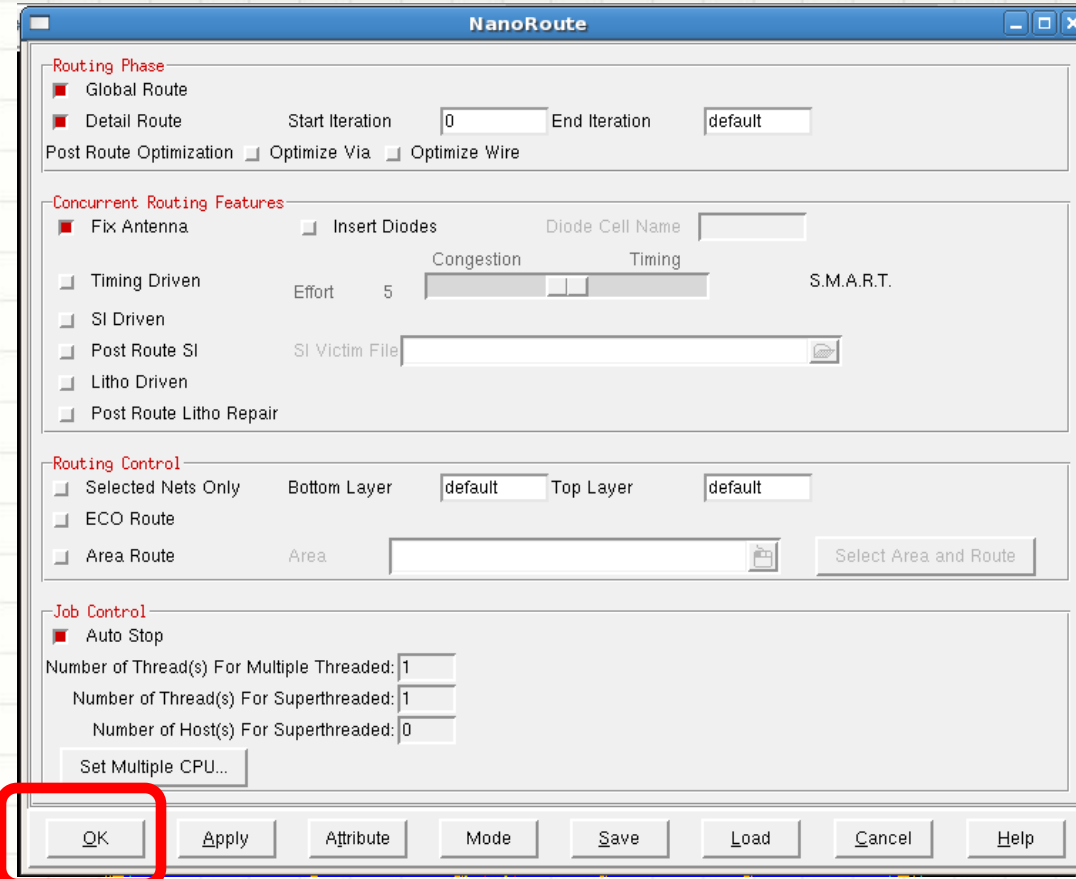


Clock Tree Synthesis

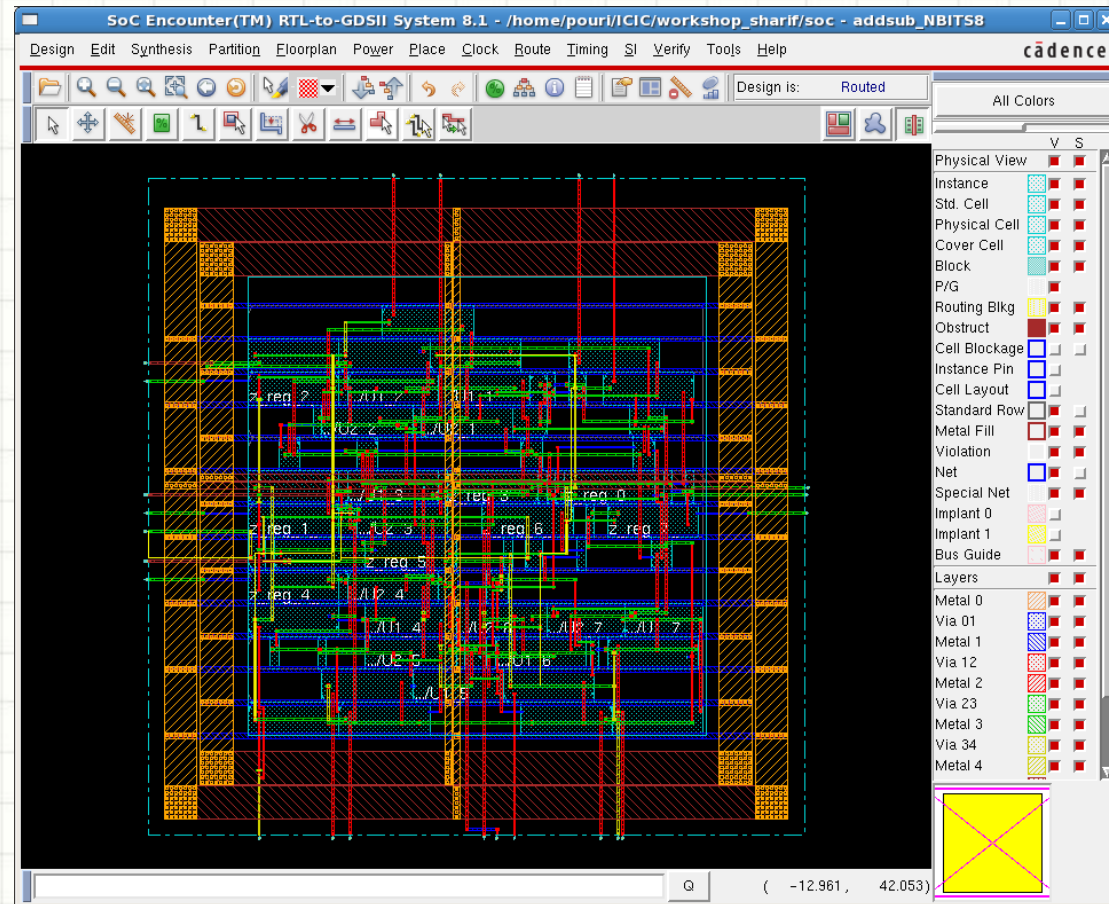


Design Routing

Route -> NanoRoute -> Route

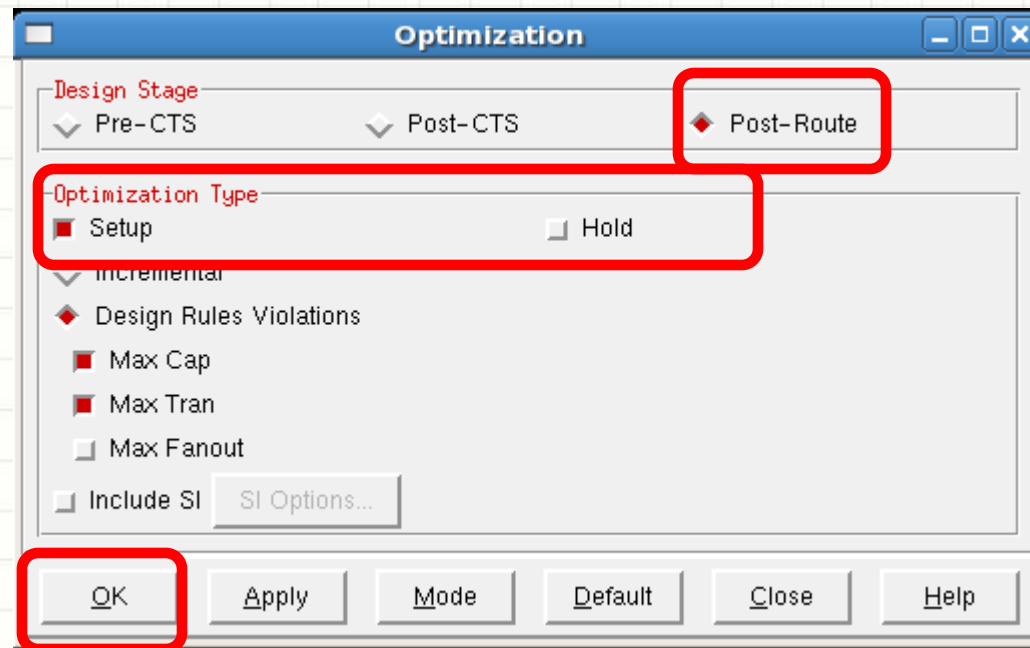


Design Routing



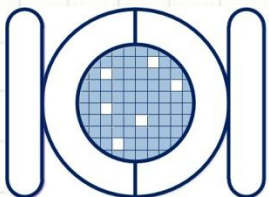
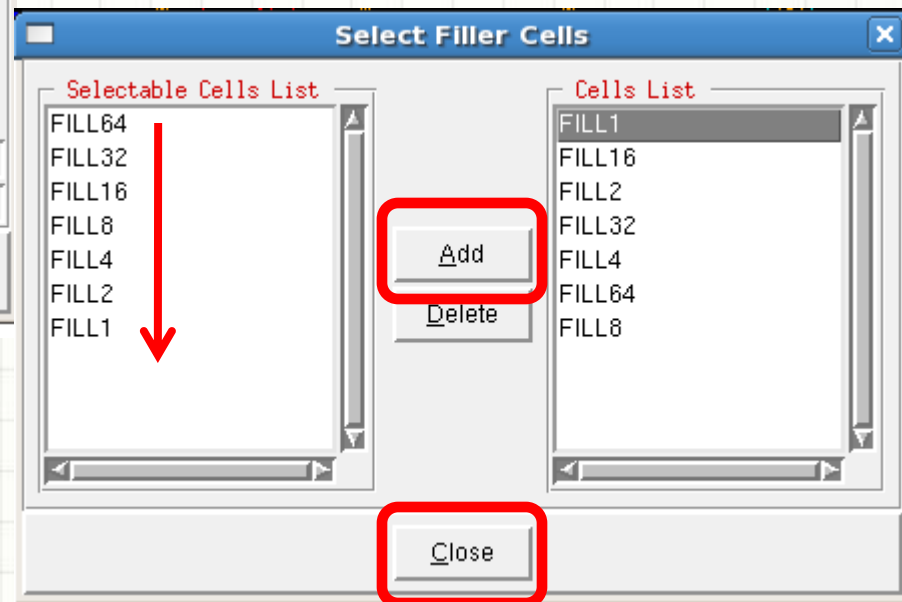
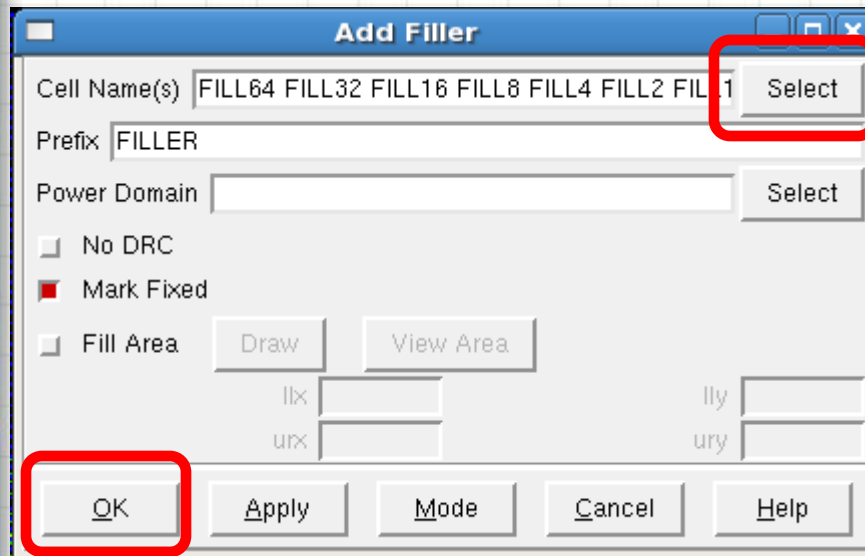
Post-Routing Timing Optimization and Analysis

Timing -> Optimize...

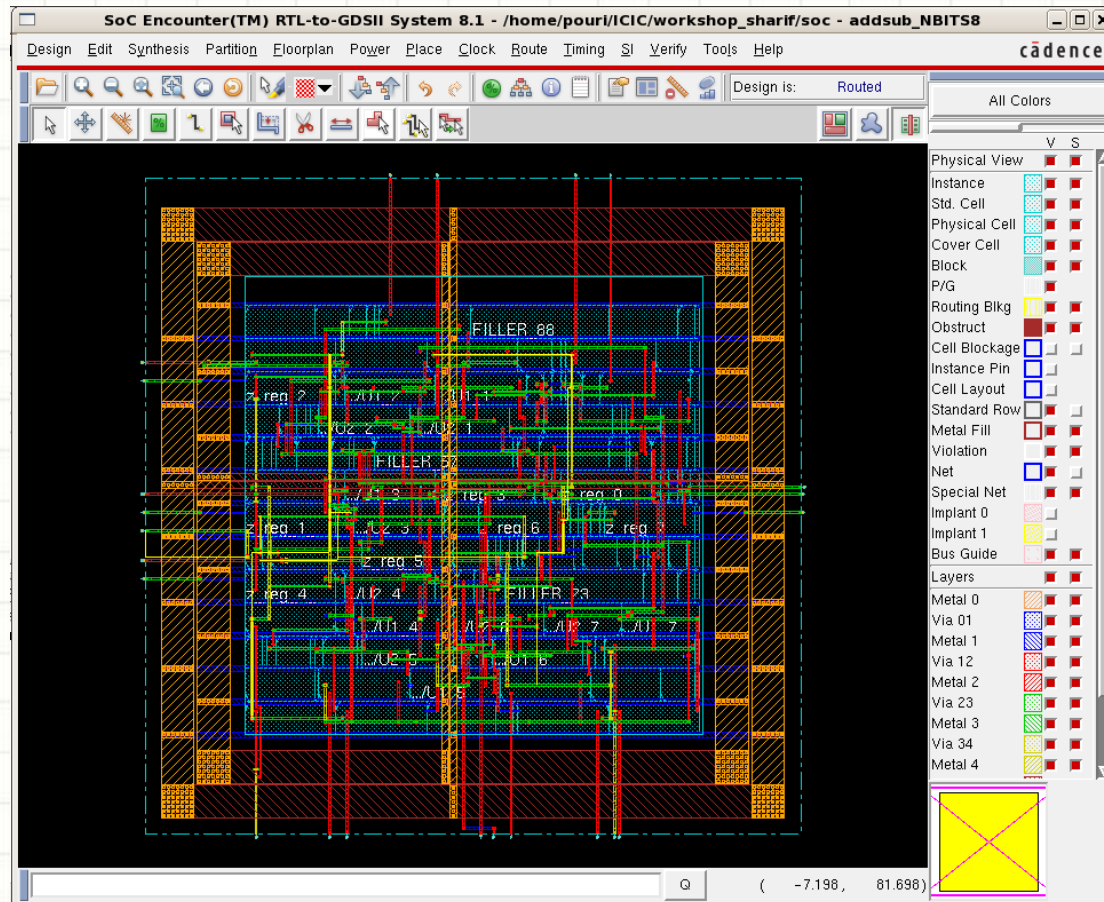


Filler Cell Placement

Place -> Physical Cells -> Add Filler...

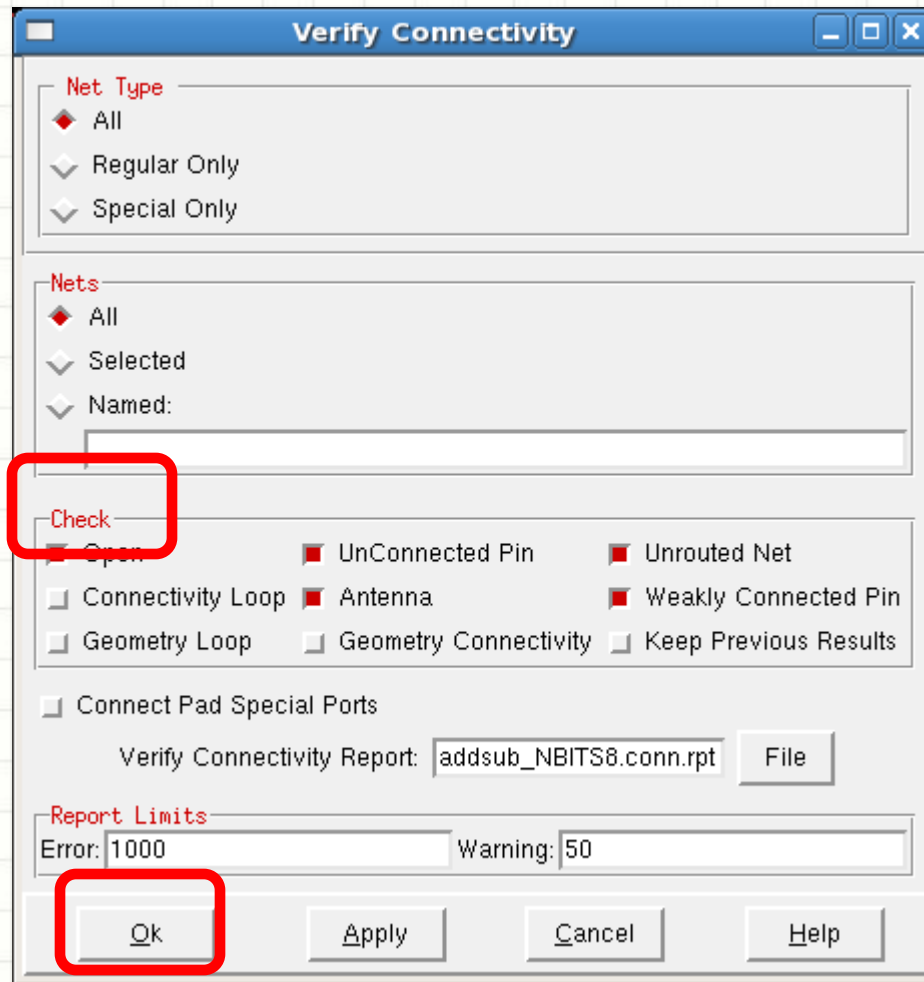


Filler Cell Placement



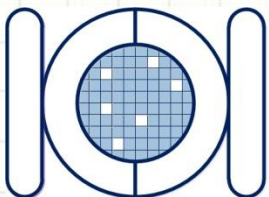
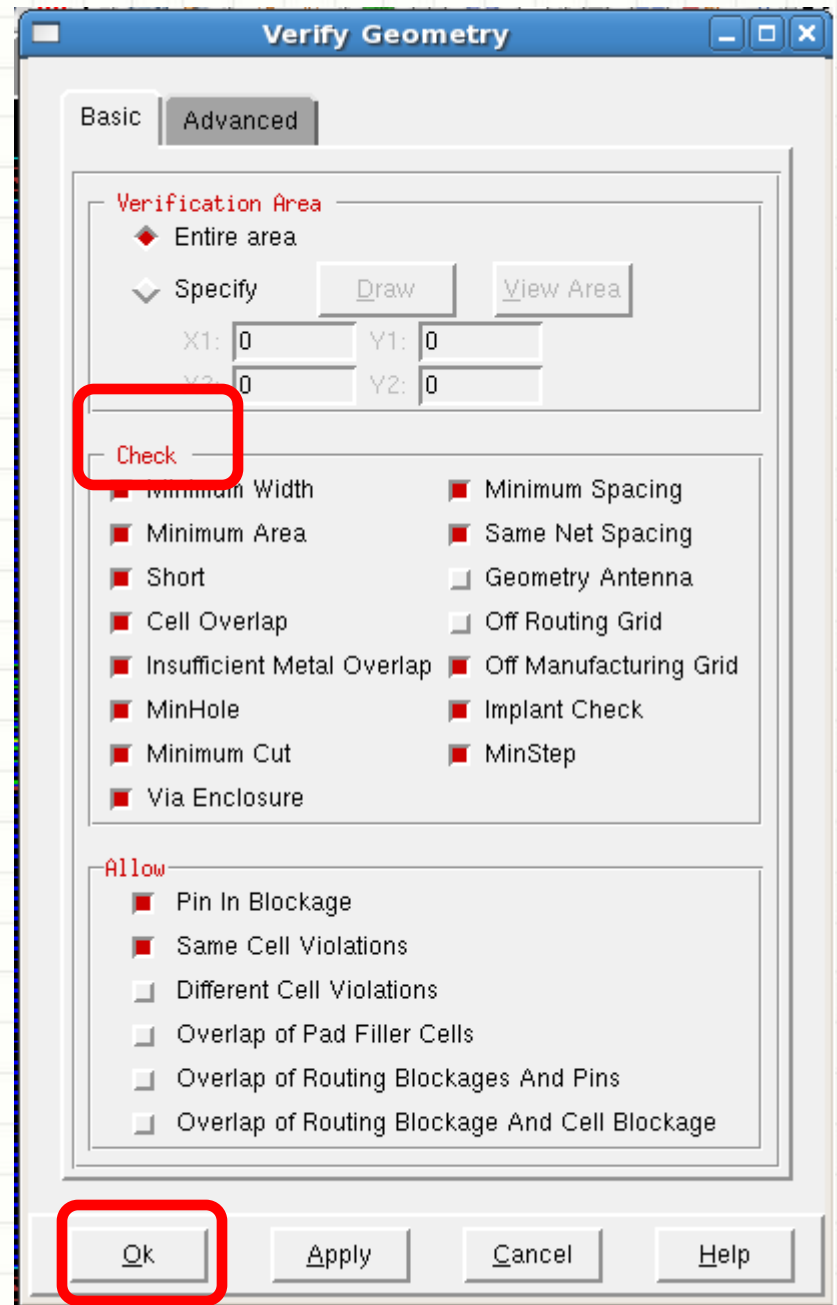
Design Checks

Verify -> Verify Connectivity...



Design Checks

Verify -> Verify Geometry...



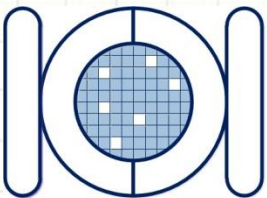
Report Generation

Design -> Report -> Netlis Statistics...

```
encounter 1> *** Statistics for net list addsub_NBITS8 ***
Number of cells      = 1774
Number of nets       = 104
Number of tri-nets   = 0
Number of degen nets = 0
Number of pins       = 289
Number of i/os       = 27
```

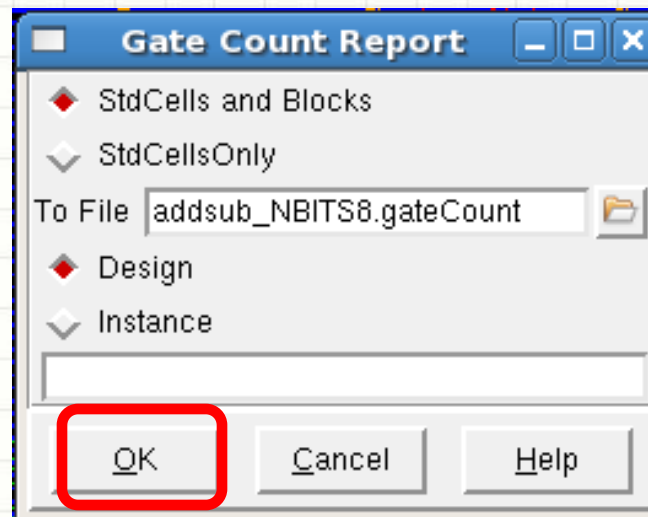
```
Number of nets with 2 terms = 78 (75.0%)
Number of nets with 3 terms = 16 (15.4%)
Number of nets with 4 terms = 2 (1.9%)
Number of nets with 5 terms = 1 (1.0%)
Number of nets with 9 terms = 4 (3.8%)
Number of nets with >=10 terms = 3 (2.9%)
```

```
*** 17 Primitives used:
Primitive XOR3X2 (2 insts)
Primitive ADDFX2 (12 insts)
Primitive AND2X2 (1 insts)
Primitive AOI22X1 (8 insts)
Primitive CLKBUFX2 (4 insts)
Primitive DFFRHQX1 (24 insts)
Primitive INVX1 (19 insts)
Primitive OR2X2 (1 insts)
Primitive XNOR2X1 (1 insts)
Primitive XOR2X1 (1 insts)
Primitive FILL1 (40 insts)
Primitive FILL16 (120 insts)
Primitive FILL2 (41 insts)
Primitive FILL32 (28 insts)
Primitive FILL4 (136 insts)
Primitive FILL64 (1209 insts)
Primitive FILL8 (127 insts)
*****
```



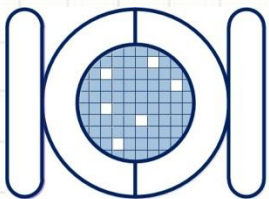
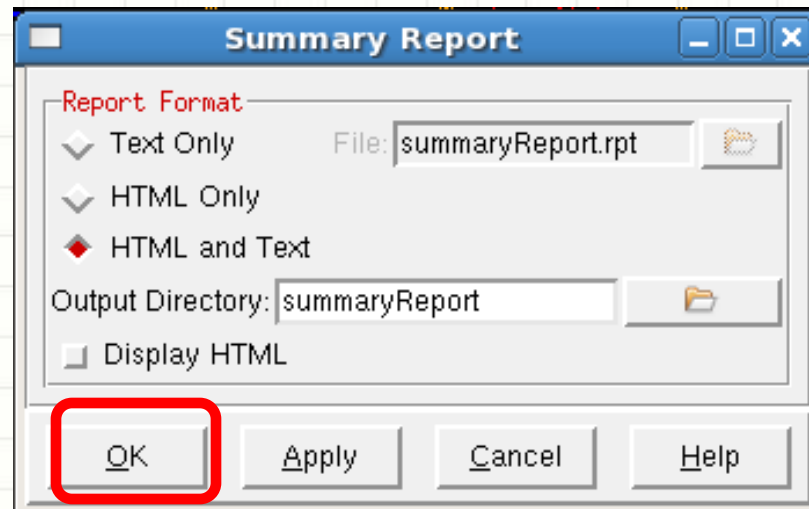
Report Generation

Design -> Report -> Gate Count...



Report Generation

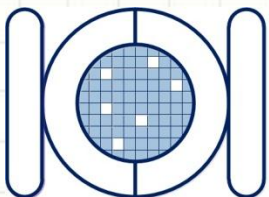
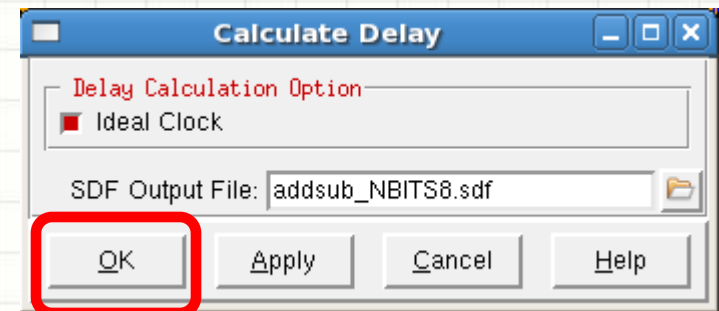
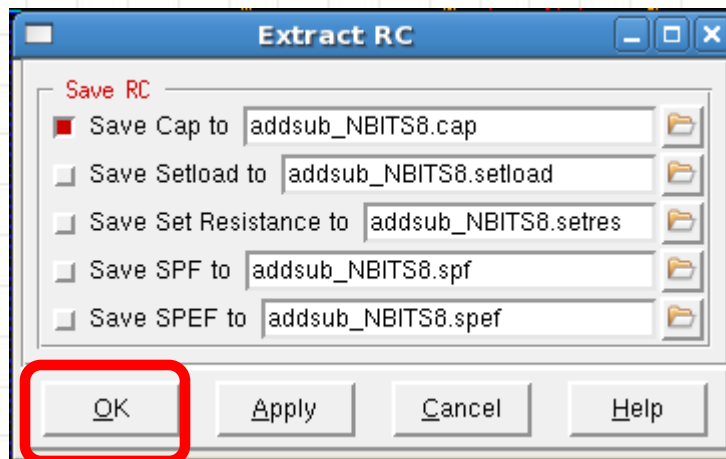
Design -> Report -> Summary...



Post-Route Timing Data Extraction

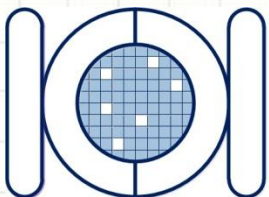
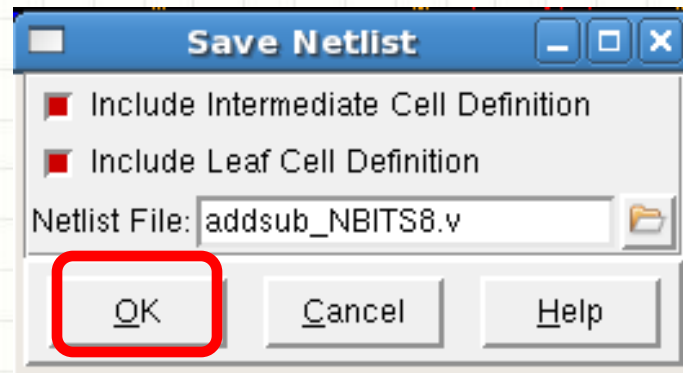
Timing -> Extract RC...

Timing -> Calculate Delay...



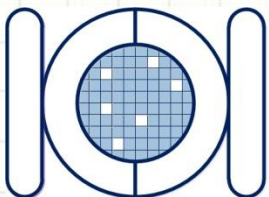
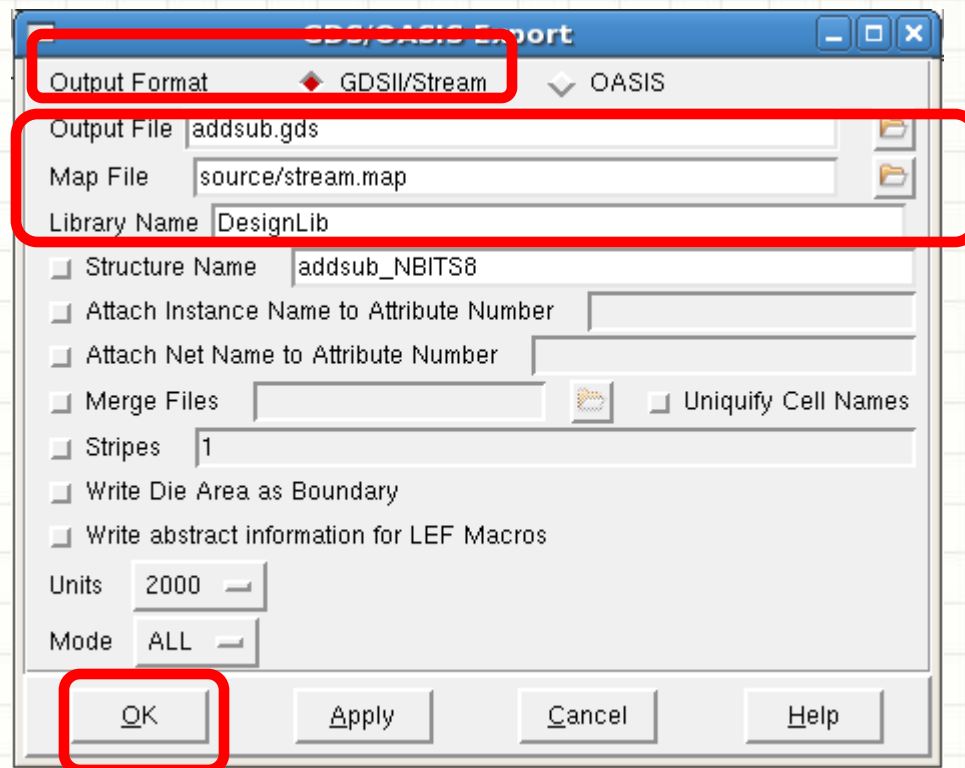
Post-Route Netlist Generation


Design -> Save -> Netlist



GDSII File Generation

Design -> Save -> GDS/OASIS



A decorative graphic consisting of several overlapping, wavy blue lines that flow from the top left towards the bottom right. The lines have a gradient from light blue to a darker blue and are set against a light gray grid background.

**Thanks For your
Attention**