Topic 3

CMOS Fabrication Process

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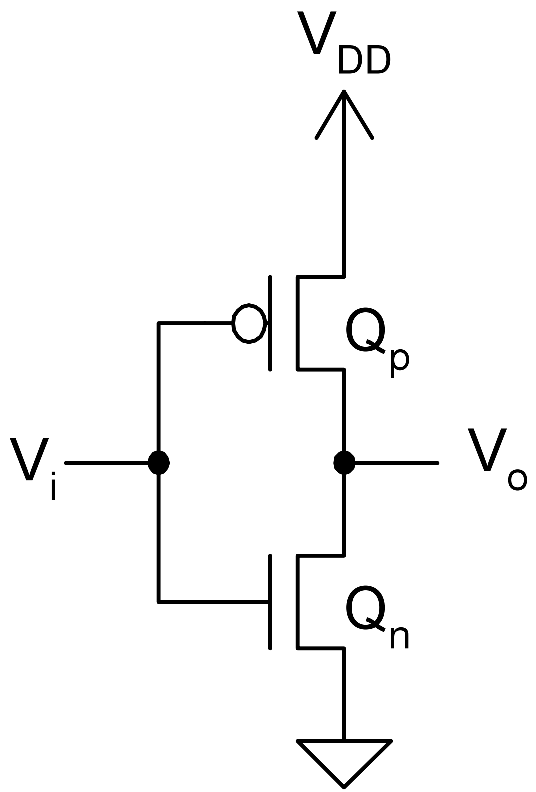
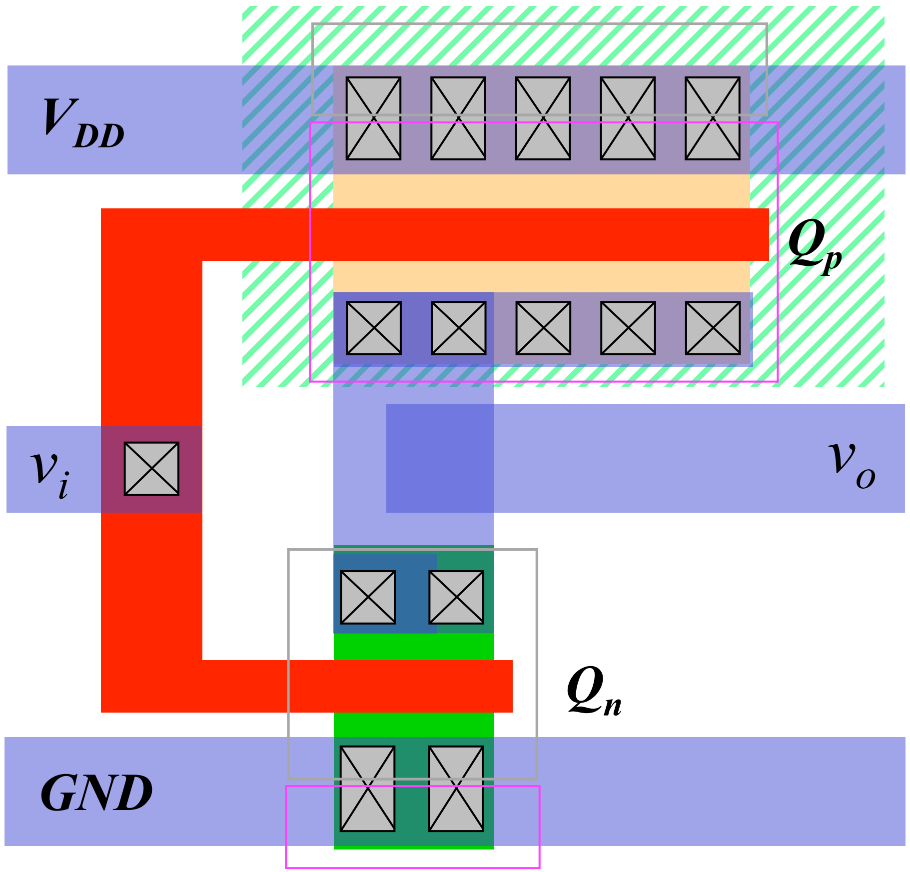
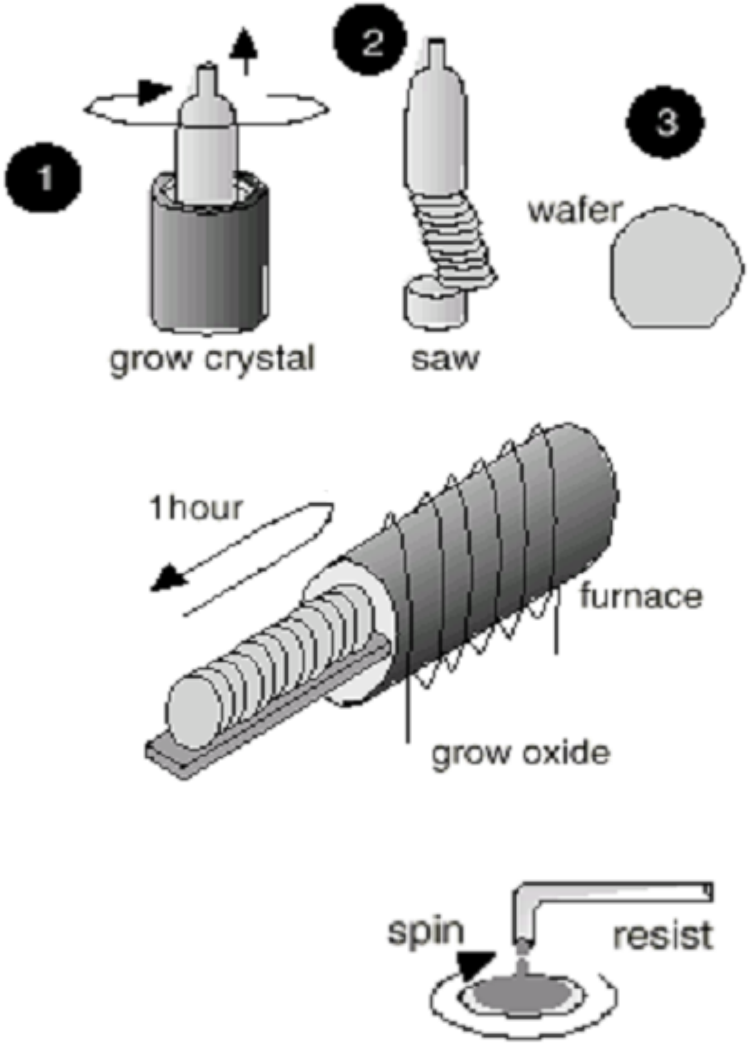
Layout of a Inverter



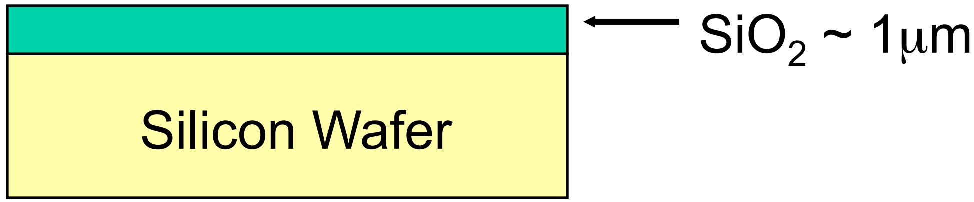


The CMOS Process - photolithography (1)

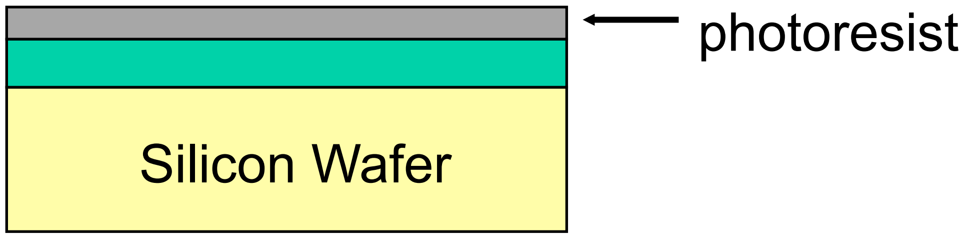


(a) Bare silicon wafer

(b) Grow Oxide layer

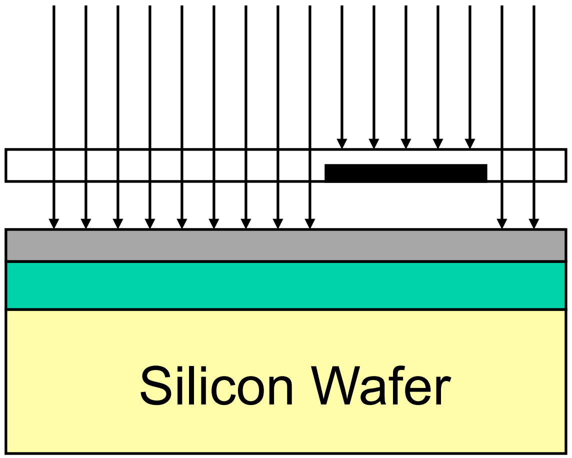


(c) Spin on photoresist

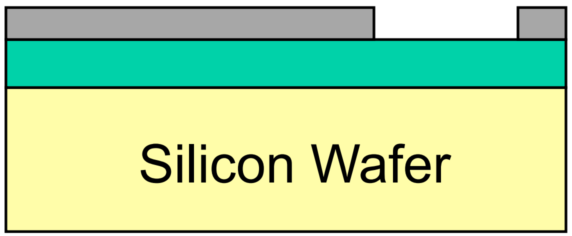


The CMOS Process - photolithography (2)

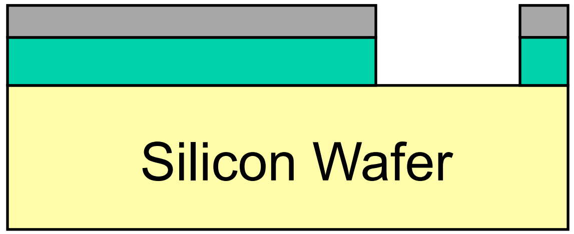
(d) Expose resist to UV light through a MASK



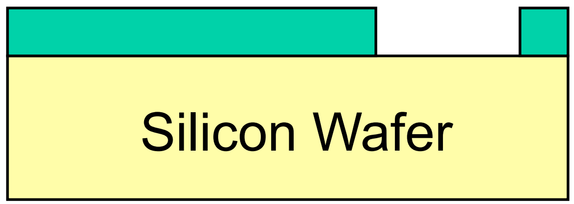
(e) Remove unexposed resist



(f) Etch away oxide

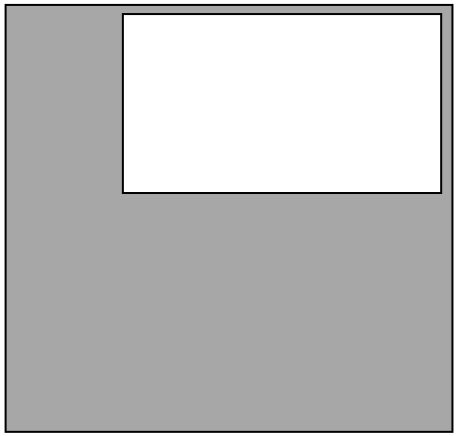


(g) Remove remaining resist

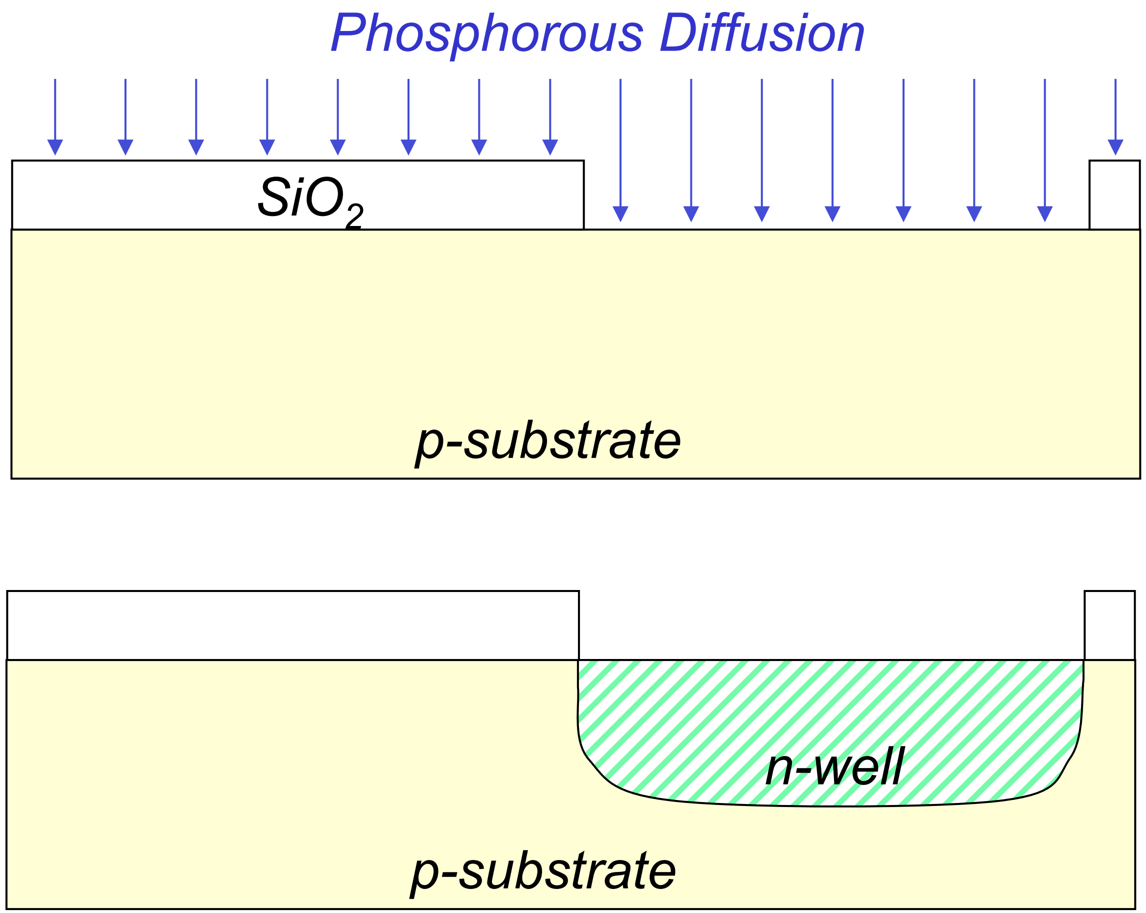


Mask 1: N-well Diffusion

- *SiO_2* is etched using *Mask 1*.

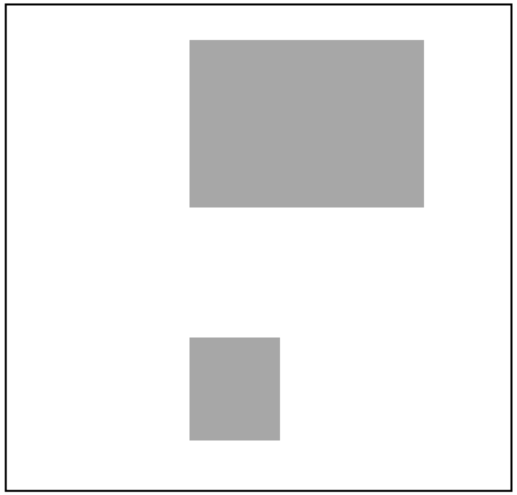


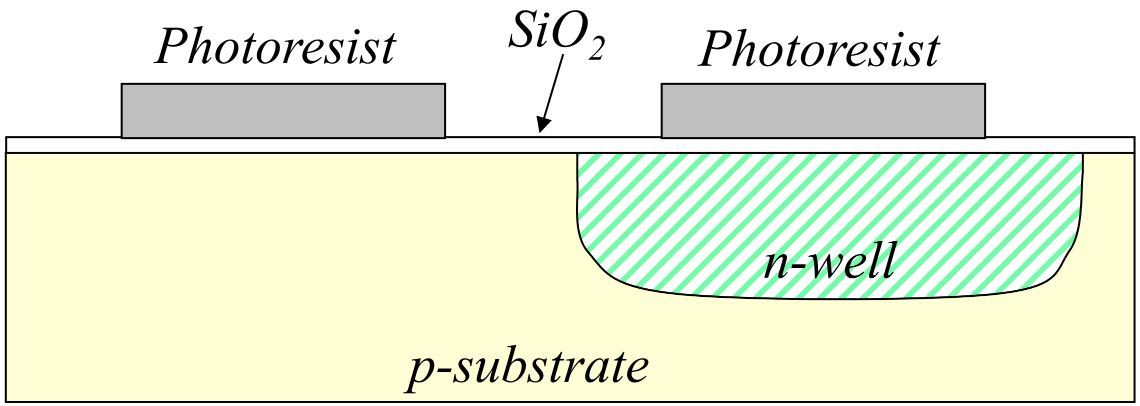
- *Phosphorous is diffused into the unmasked regions of silicon creating an n-well for the fabrication of p-channel devices*



Mask 2: Define Active Regions

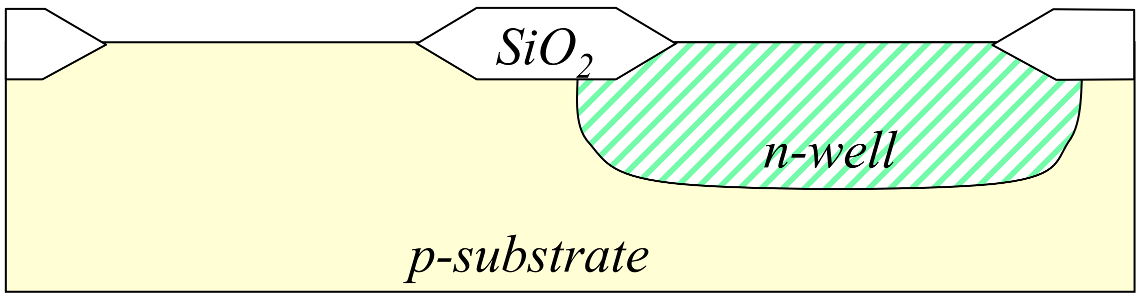
- *Mask 2 creates the active regions where the MOSFETs will be placed*





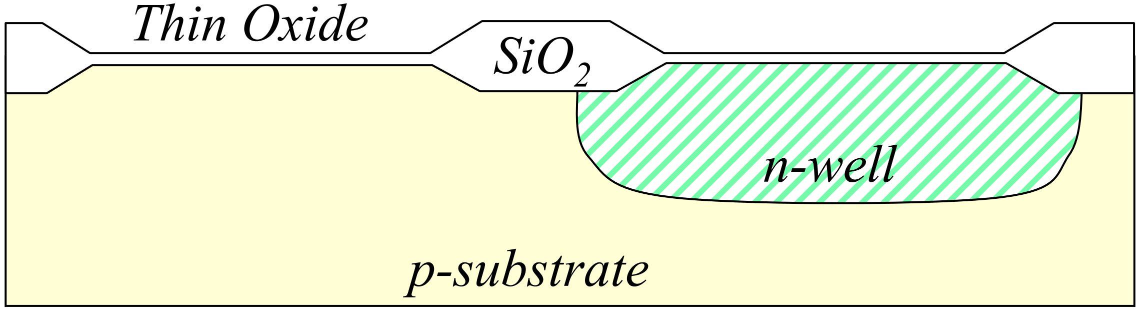
A thick field oxide is grown using a contruction technique called Local Oxidation Of Silicon (LOCOS).

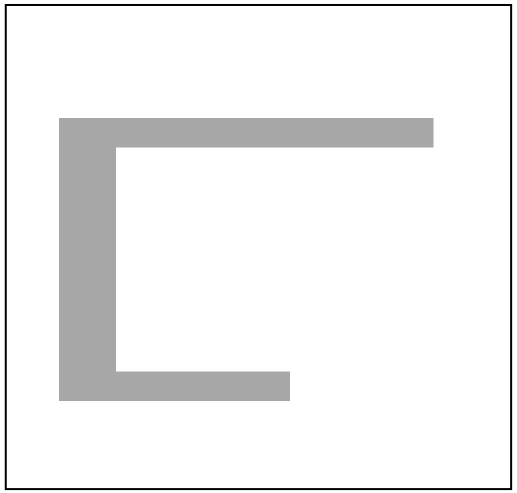
- *The thick oxide regions provides isolation between the MOSFETs*



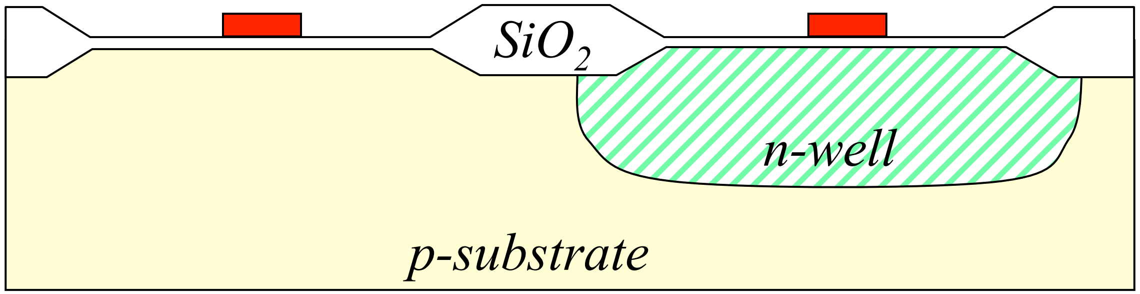
Mask 3: Polysilicon Gate

- A high quality thin oxide is grown in the active area *(~100Å->300Å)*
- *Mask 3* is used to deposit the polysilicon gate *(most critical step)*



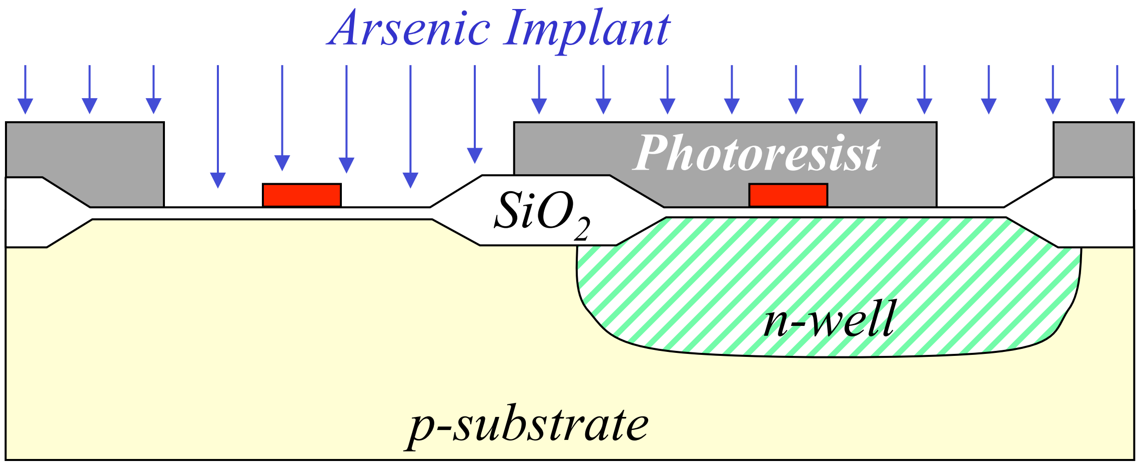


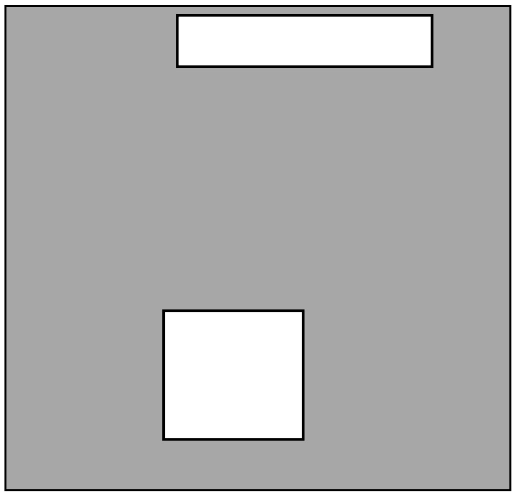
The polysilicon layer is usually arsenic doped (n-type). The photolithography in this step is the most demanding since it requires the finest resolution to create the narrow MOS channels.



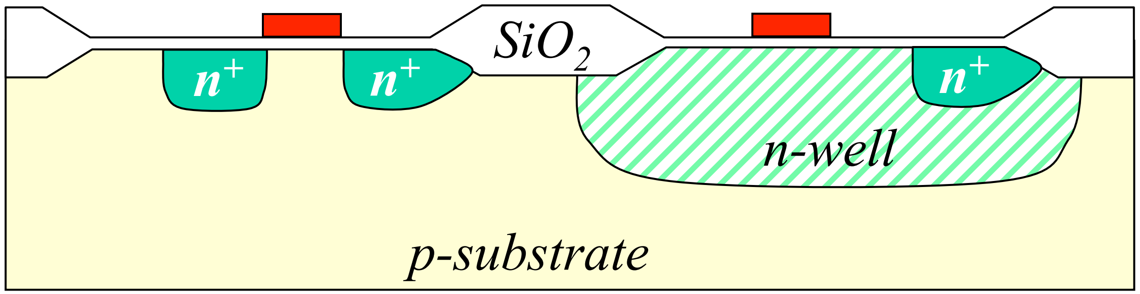
Mask 4: n+ Diffusion

- *Mask 4* is used to control a heavy arsenic implant and create the source and drain of the n-channel devices.
- This is a **self-aligned** structure.



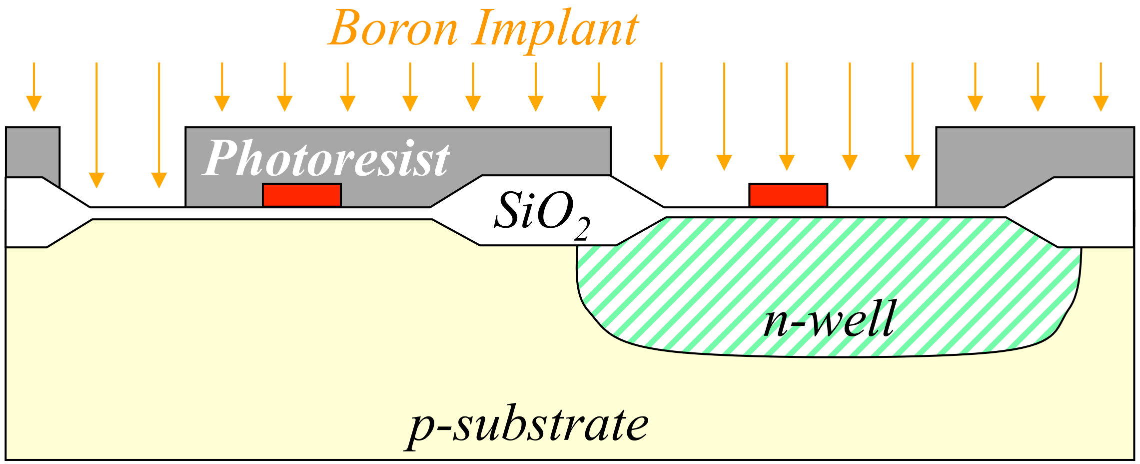


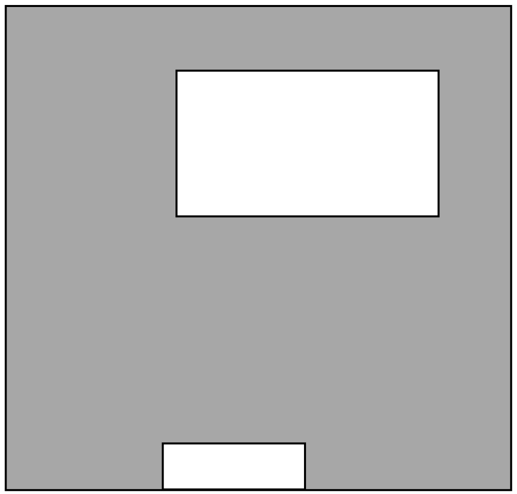
The polysilicon gate acts like a barrier for this implant to protect the channel region.



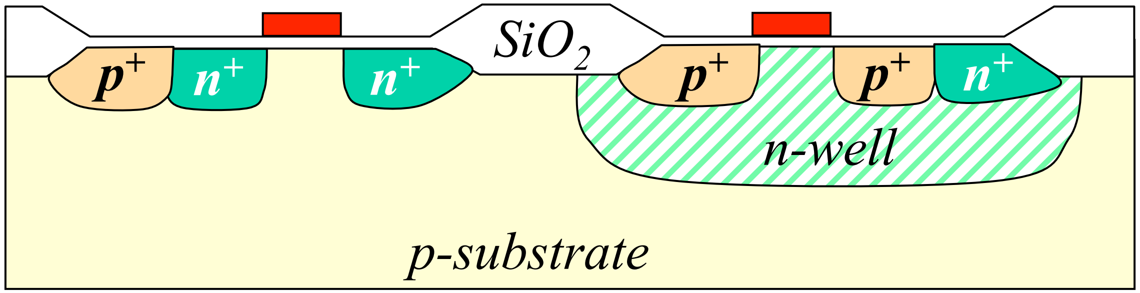
Mask 5: p+ Diffusion

- *Mask 5* is used to control a heavy Boron implant and create the source and drain of the n-channel devices.
- This is a self-aligned structure.



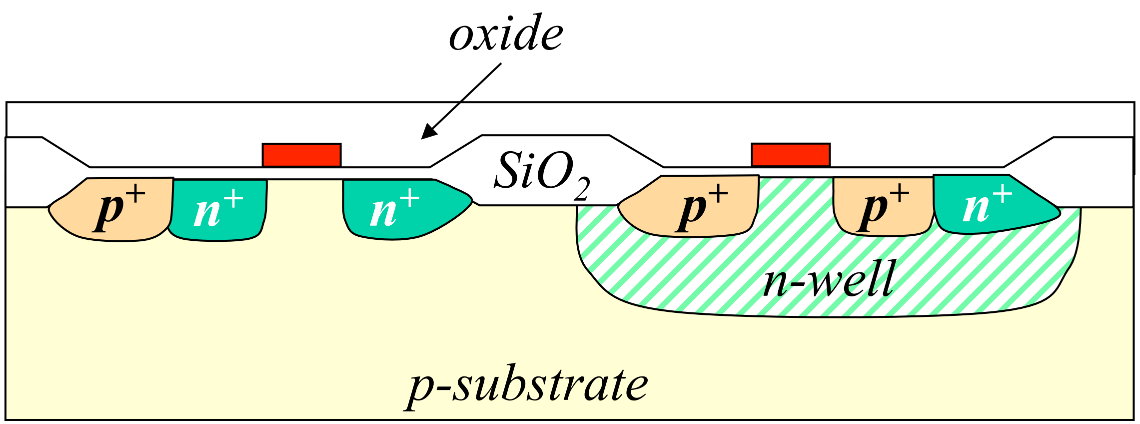


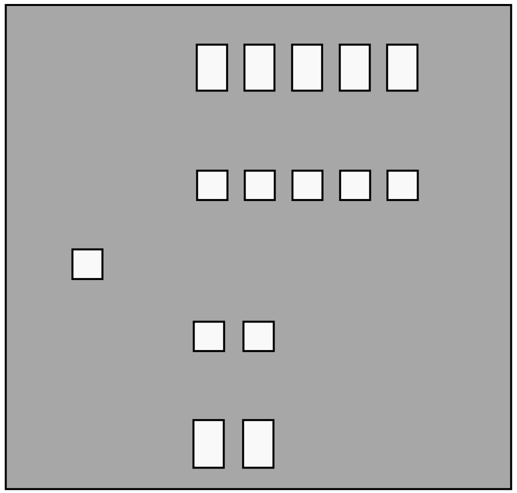
The polysilicon gate acts like a barrier for this implant to protect the channel region.

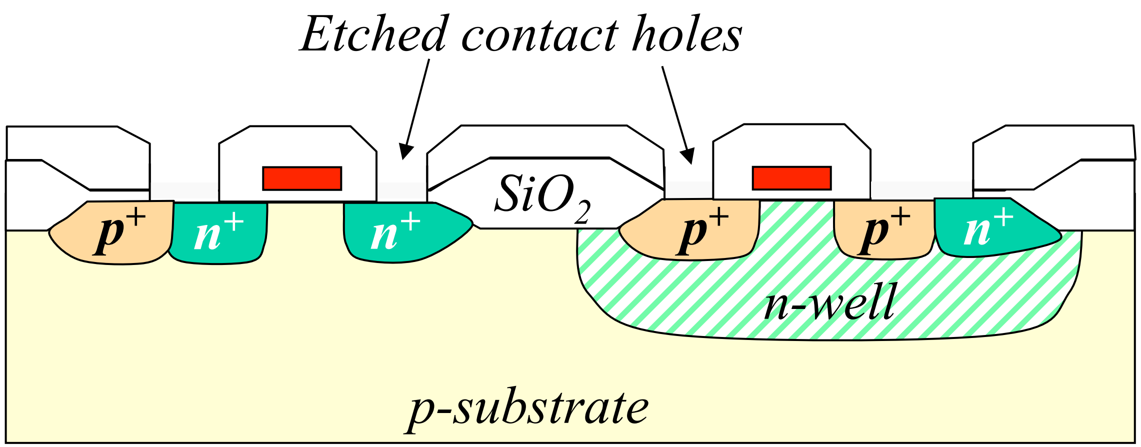


Mask 6: Contact Holes

- A thin layer of oxide is deposited over the entire wafer
- *Mask 6* is used to pattern the contact holes
- Etching opens the holes.

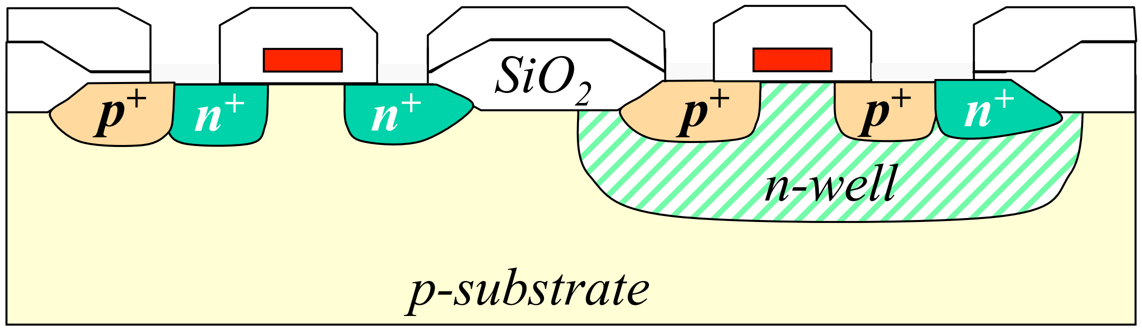


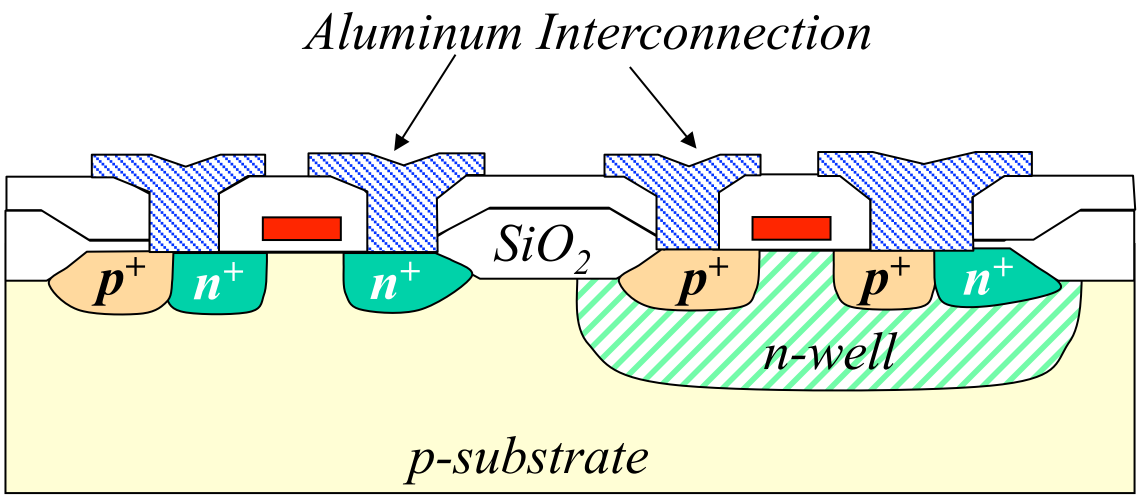




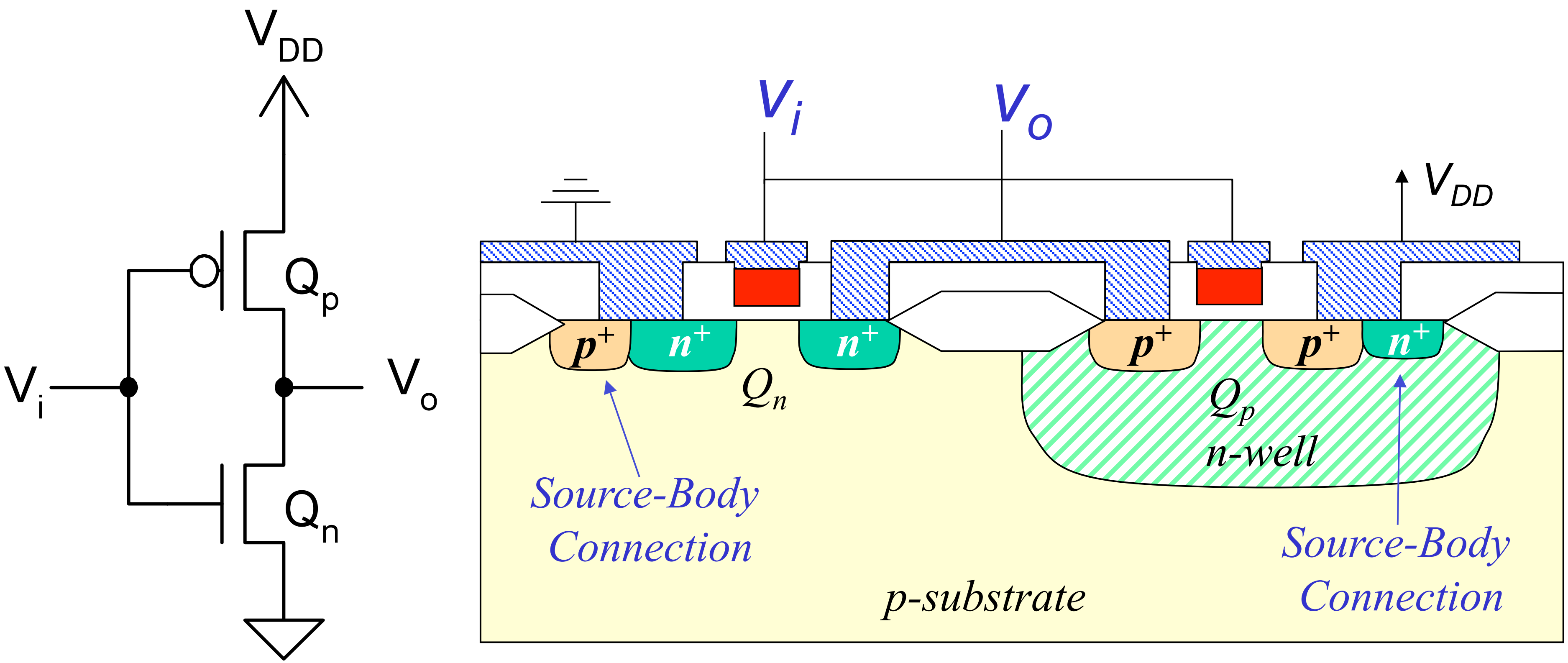
Mask 7: Metalization

- A thin layer of aluminum is evaporated or sputtered onto the wafer.
- *Mask 7* is used to pattern the interconnection.



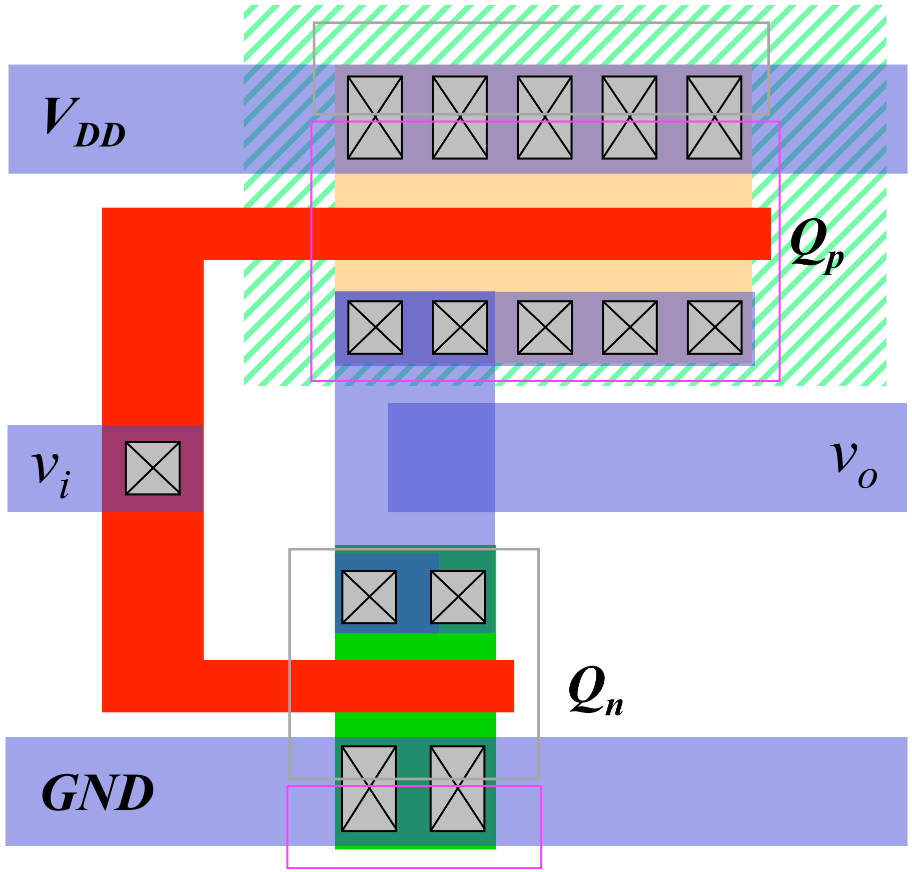


Cross section of a CMOS Inverter

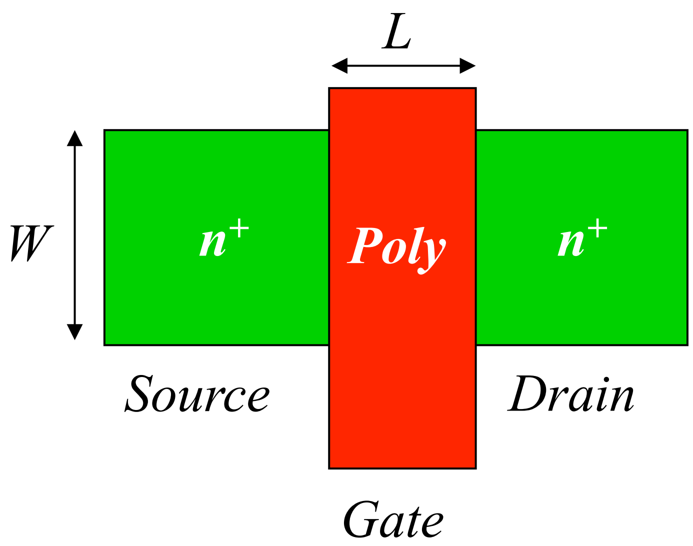


Physical Layout of an Inverter

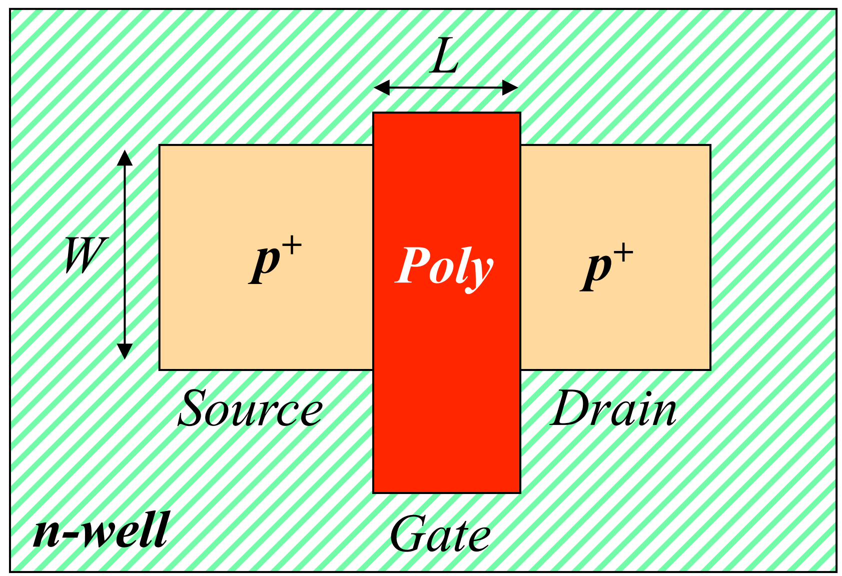
- *n-well*
- *PMOS active region*
- *NMOS active region*
- *n^+ diffusion*
- *p^+ diffusion*
- *Poly 1 (poly-Si gate)*
- *Contact Hole*
- *Metal 1*



Dimension of transistors

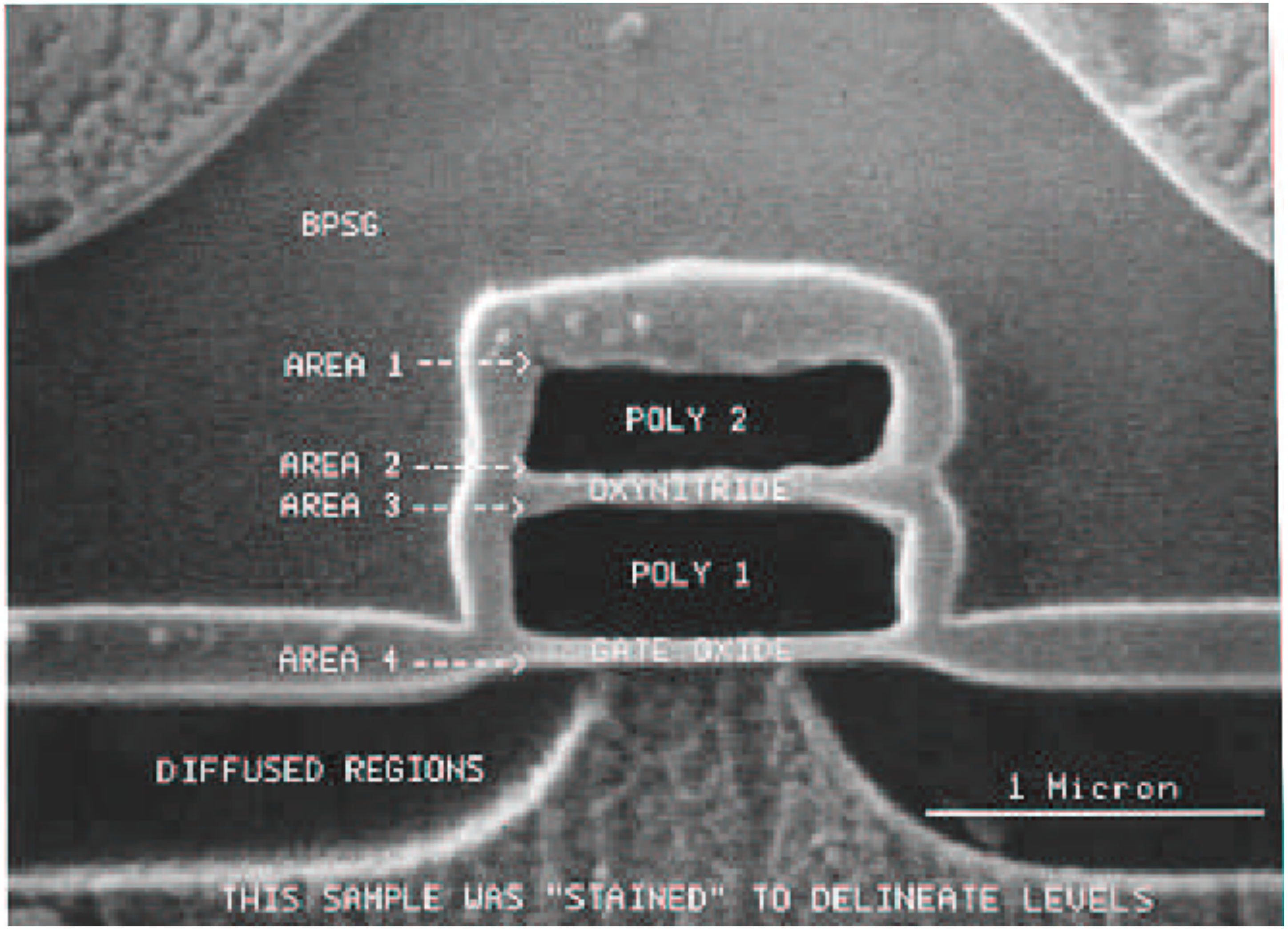


n-channel MOSFET

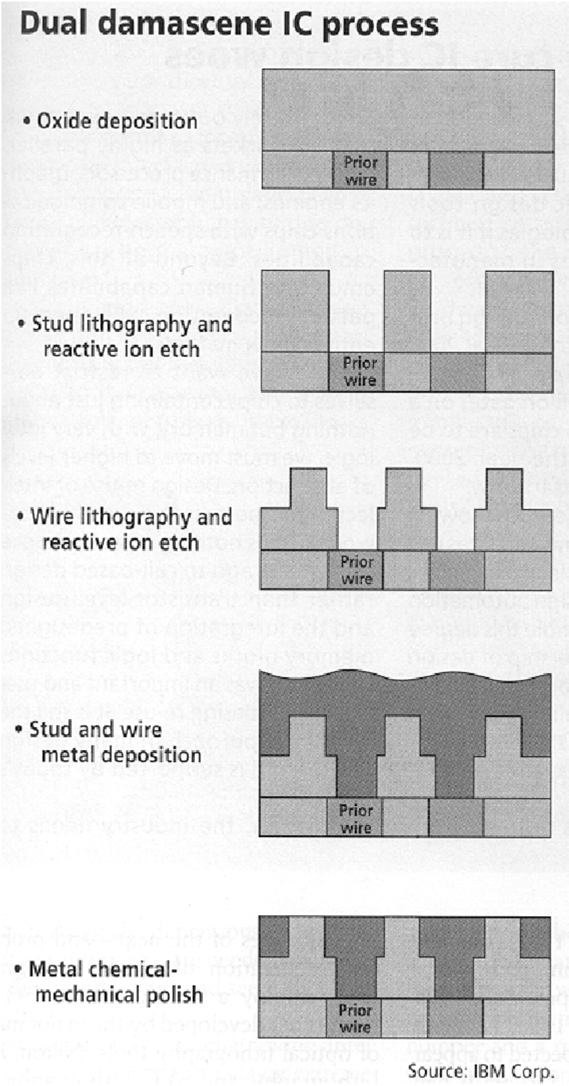


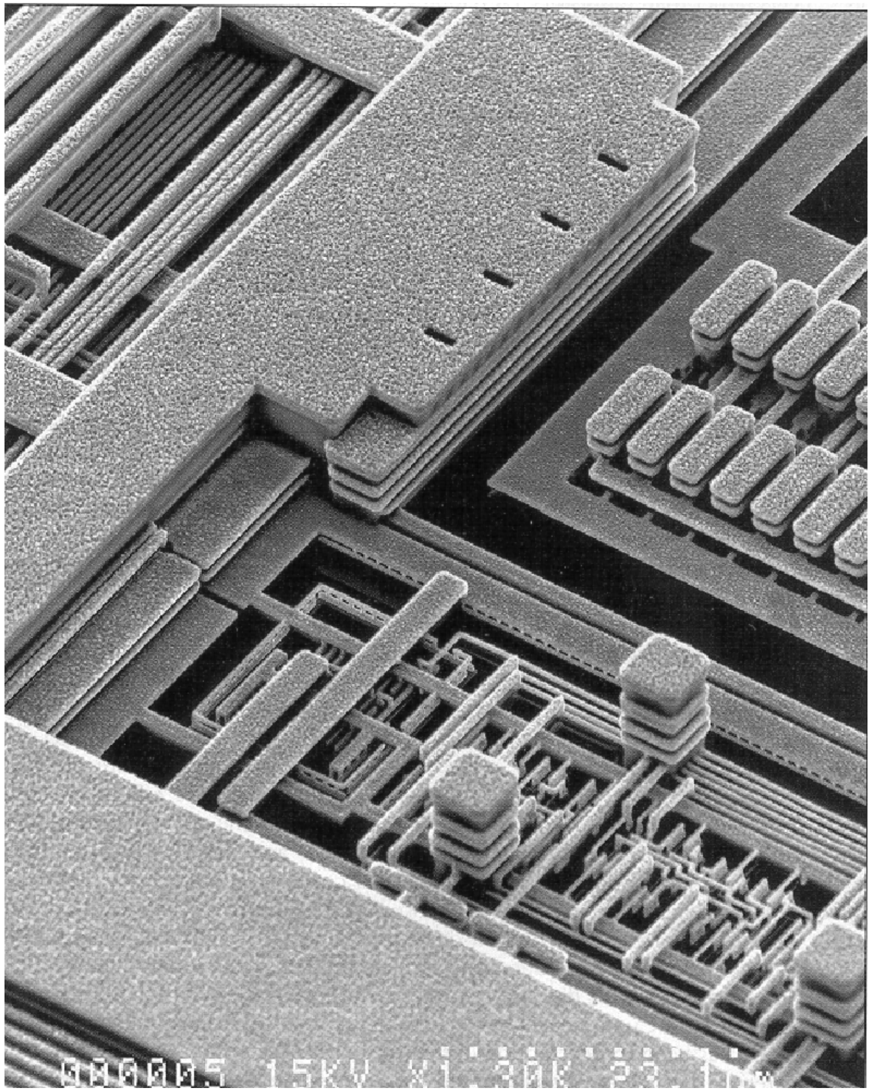
p-channel MOSFET

Photo cross-section of a transistor



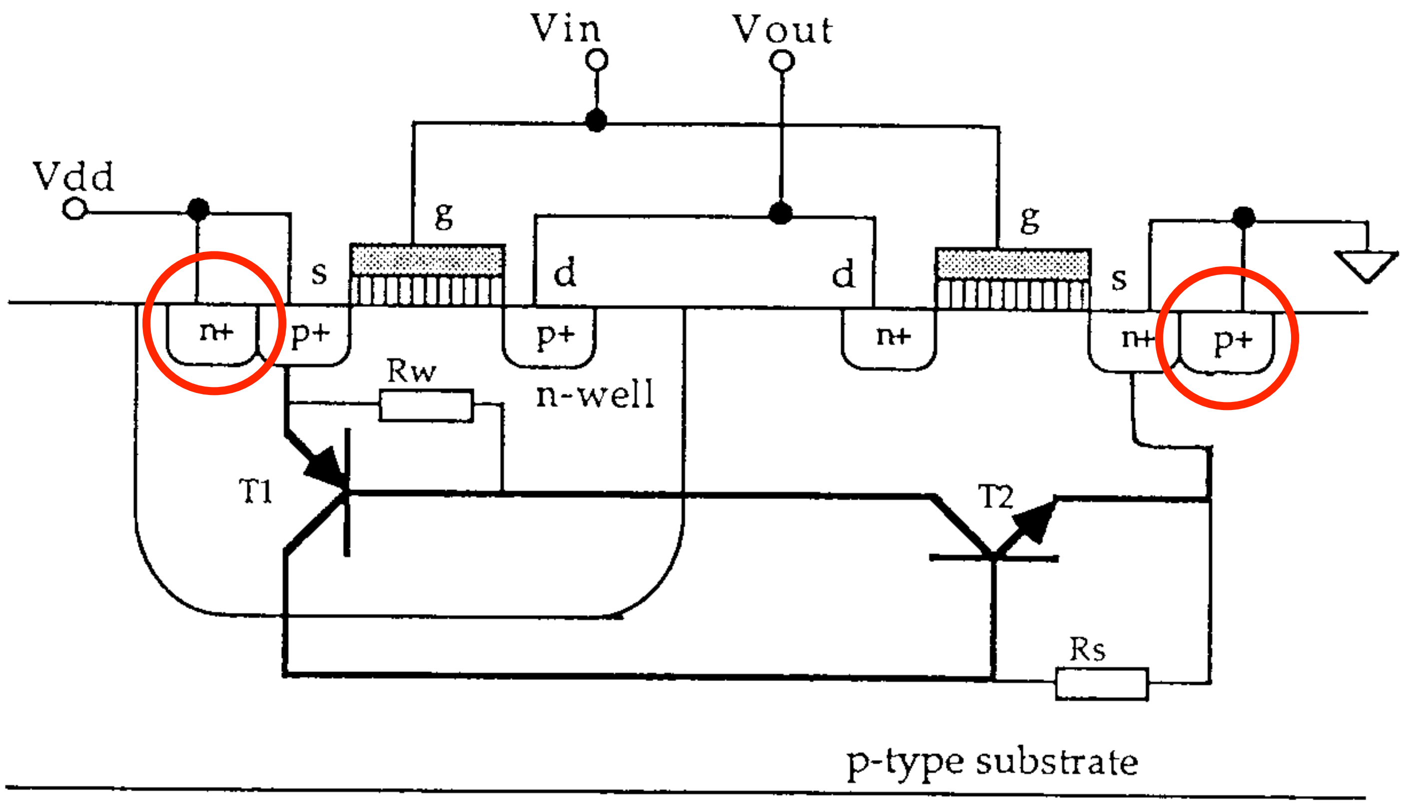
Advanced metalization with polishing





Latch-up problem (1)

- As shown above, the p+ region of the p-transistor, the n-well and the p- substrate form a parasitic pnp transistor T1.
- The n- well, the p- substrate and the p+ source of the n-transistor forms another parasitic npn transistor T2.
- There exists two resistors Rw and Rs due to the resistive drop in the well area and the substrate area.



Latch-up (con't)

- T1 and T2 form a thyristor circuit.
- If Rw and/or Rs are not 0, and for some reason (power-up, current spike etc), T1 or T2 are forced to conduct, Vdd will be shorted to Gnd through the small resistances and the transistors.
- Once the circuit is 'fired', both transistors will remain conducting due to the voltage drop across Rw and Rs. The only way to get out of this mode is to turn the power off.
- This condition is known as **latch-up**.
- To avoid latch-up, substrate-taps (tied to Gnd) and well-taps (tied to Vdd) are inserted as frequently as possible. This has the effect of shorting out Rw and Rs.