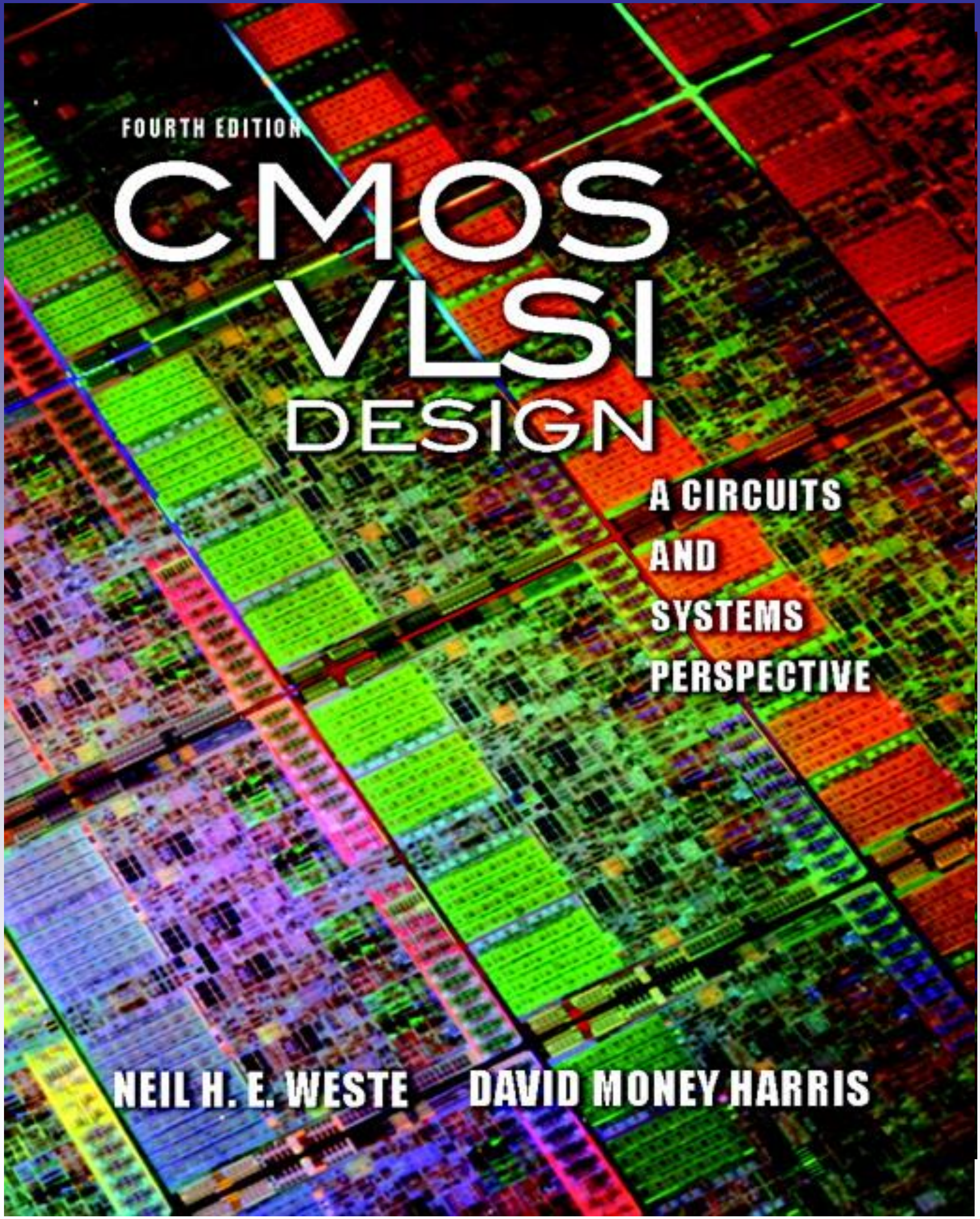
Chapter 1

Introduction



Addison-Wesley
is an imprint of
PEARSON

Digital Integrated Circuits
A Design Perspective

Jan M. Rabaey
Anantha Chandrakasan
Borivoje Nikolic

Manufacturing Process

July 30, 2002

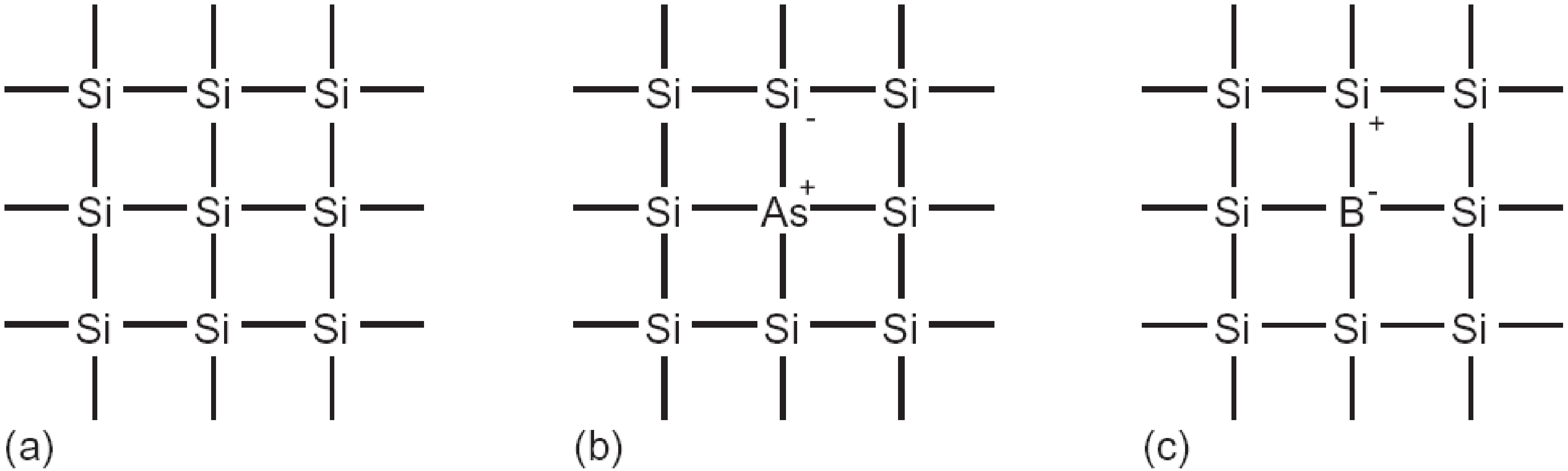


FIGURE 1.7 Silicon lattice and dopant atoms

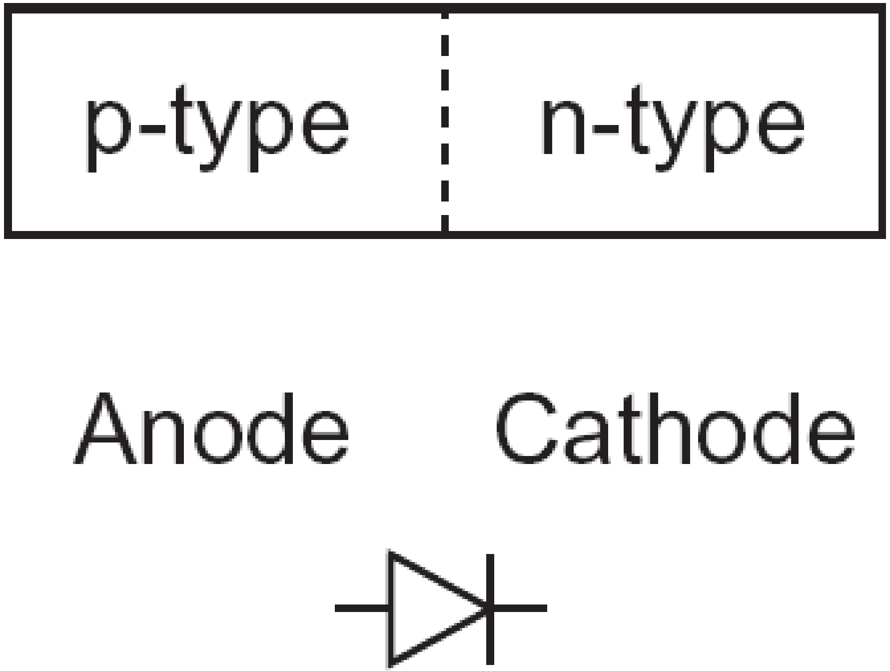


FIGURE 1.8
p-n junction diode
structure and symbol

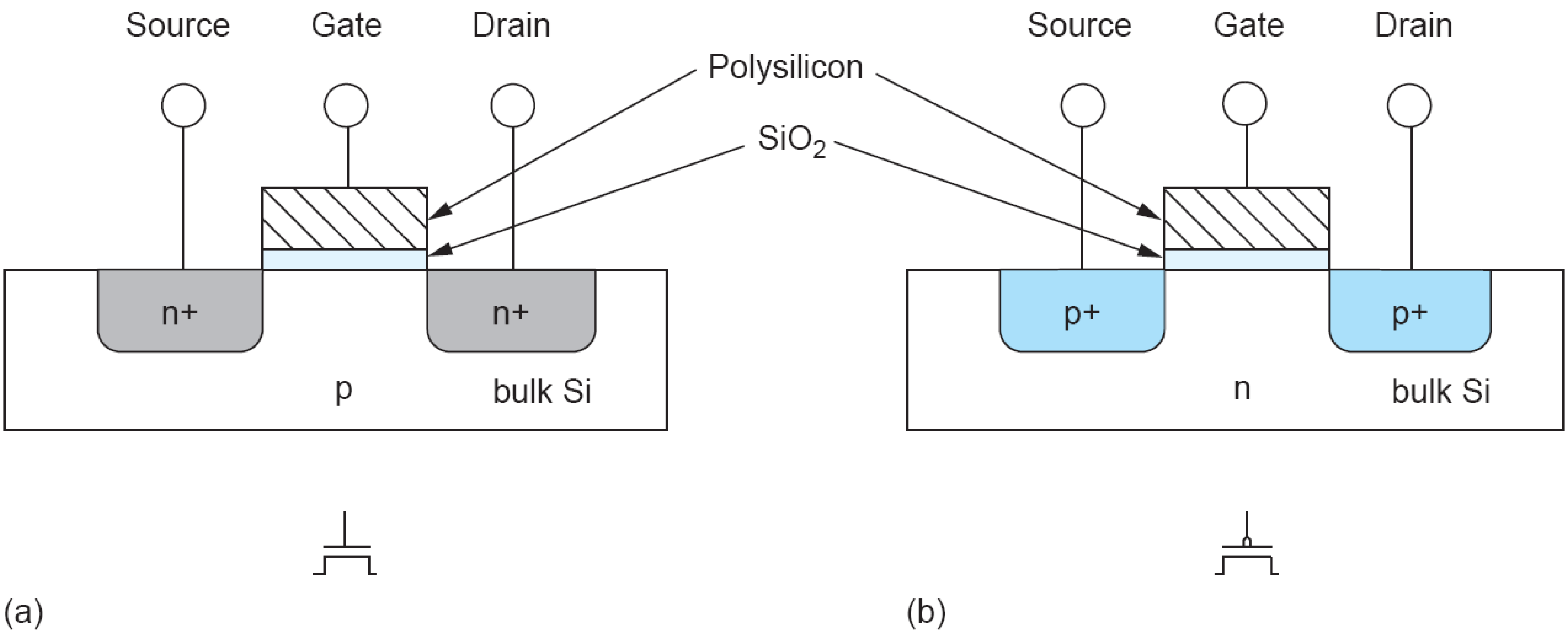


FIGURE 1.9 nMOS transistor (a) and pMOS transistor (b)

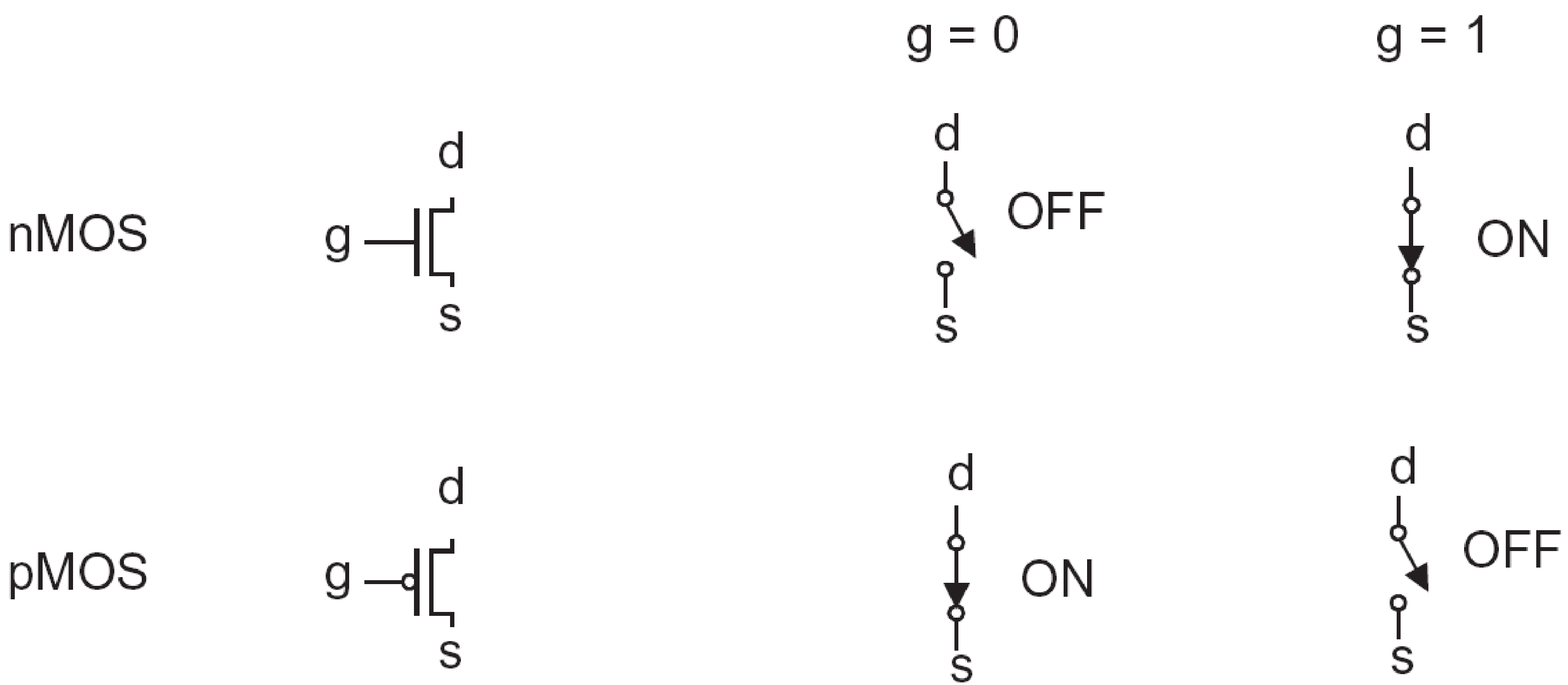


FIGURE 1.10 Transistor symbols and switch-level models

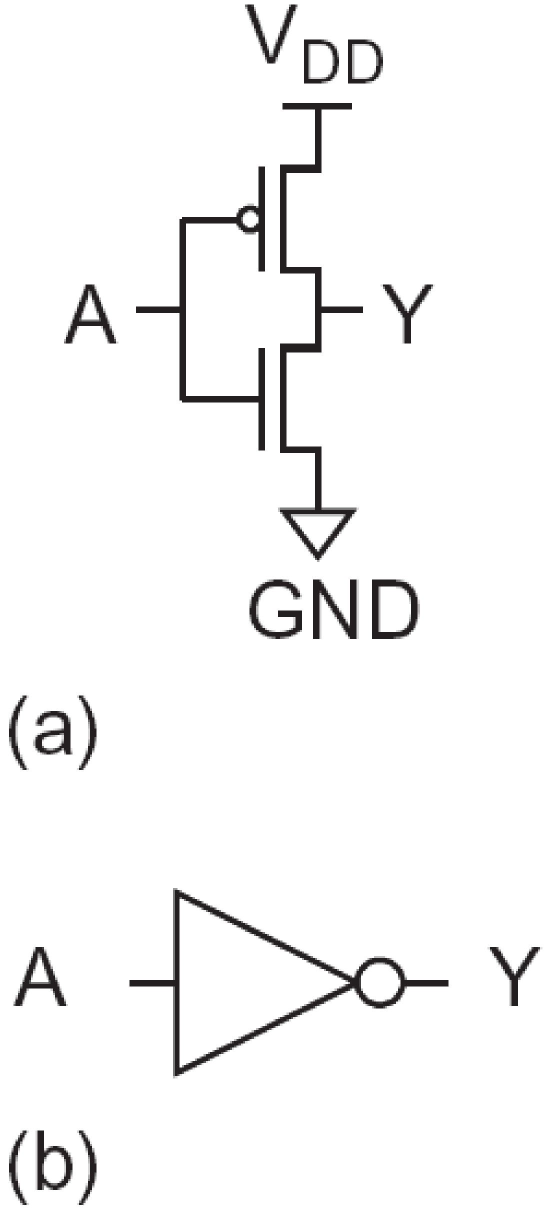
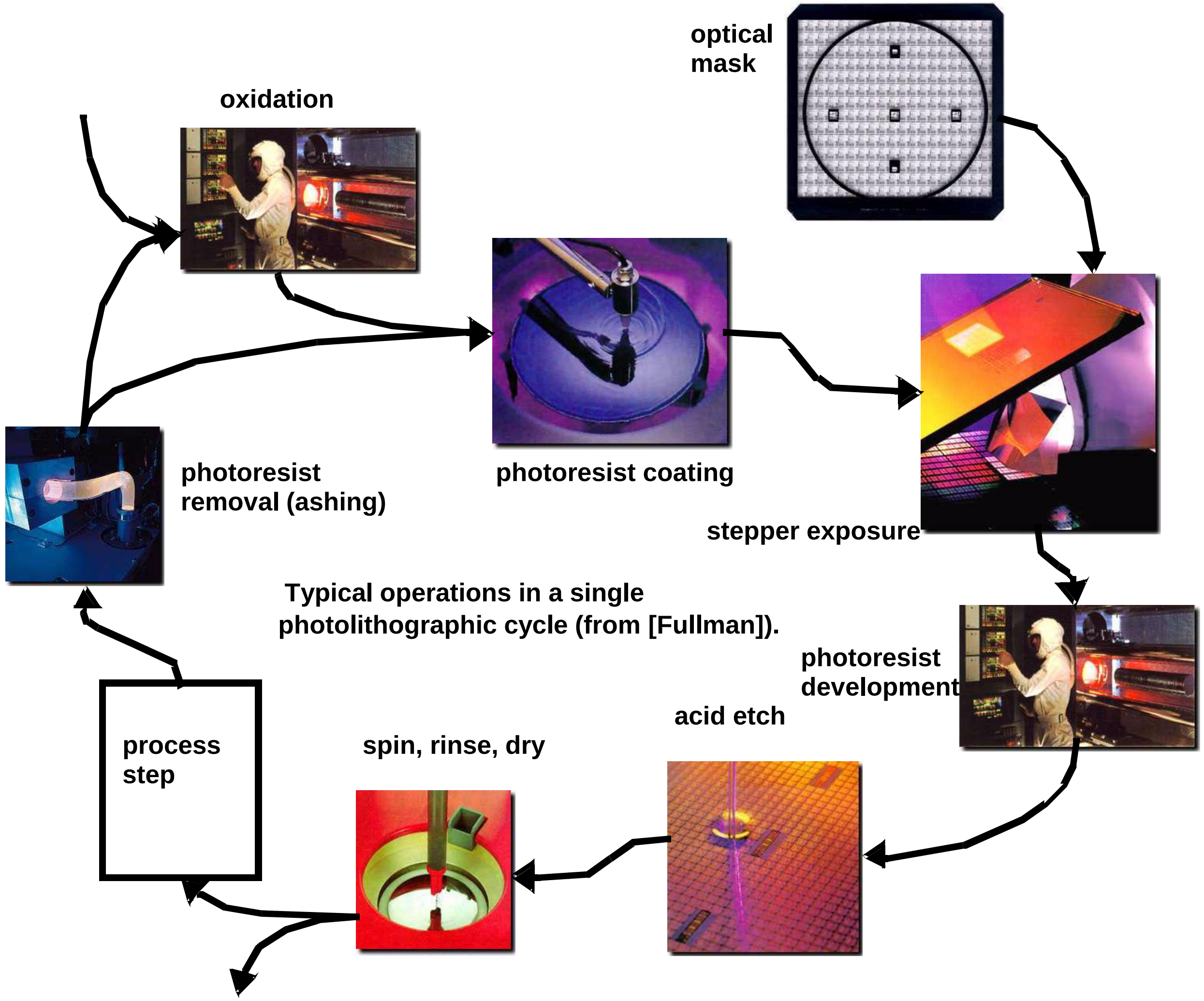


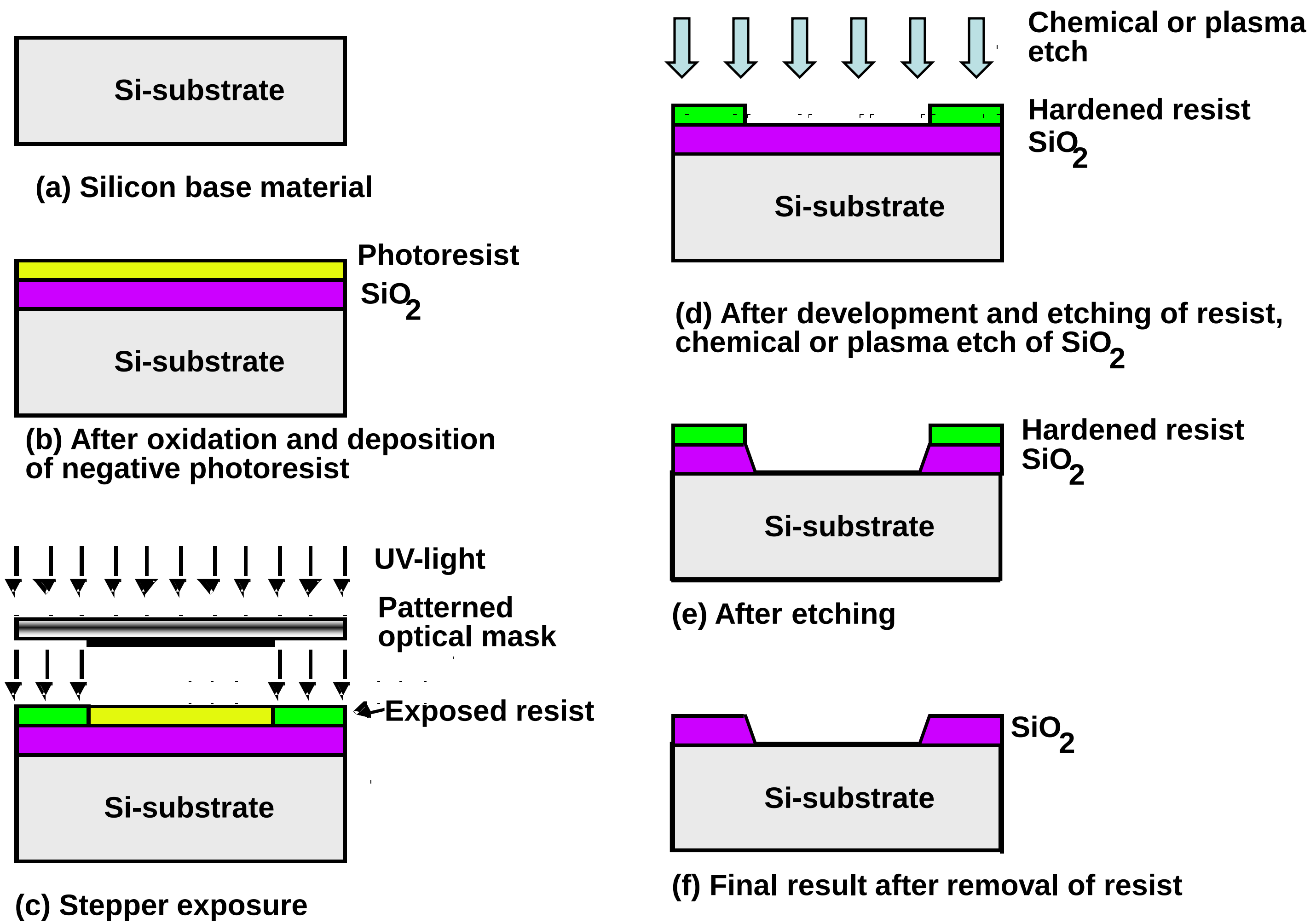
FIGURE 1.11
Inverter schematic
(a) and symbol
(b) $Y = \overline{A}$

Photo-Lithographic Process



Typical operations in a single photolithographic cycle (from [Fullman]).

Patterning of SiO2



CMOS Process at a Glance

Define active areas
Etch and fill trenches

↓

Implant well regions

↓

Deposit and pattern polysilicon layer

↓

Implant source and drain regions and substrate contacts

↓

Create contact and via windows
Deposit and pattern metal layers

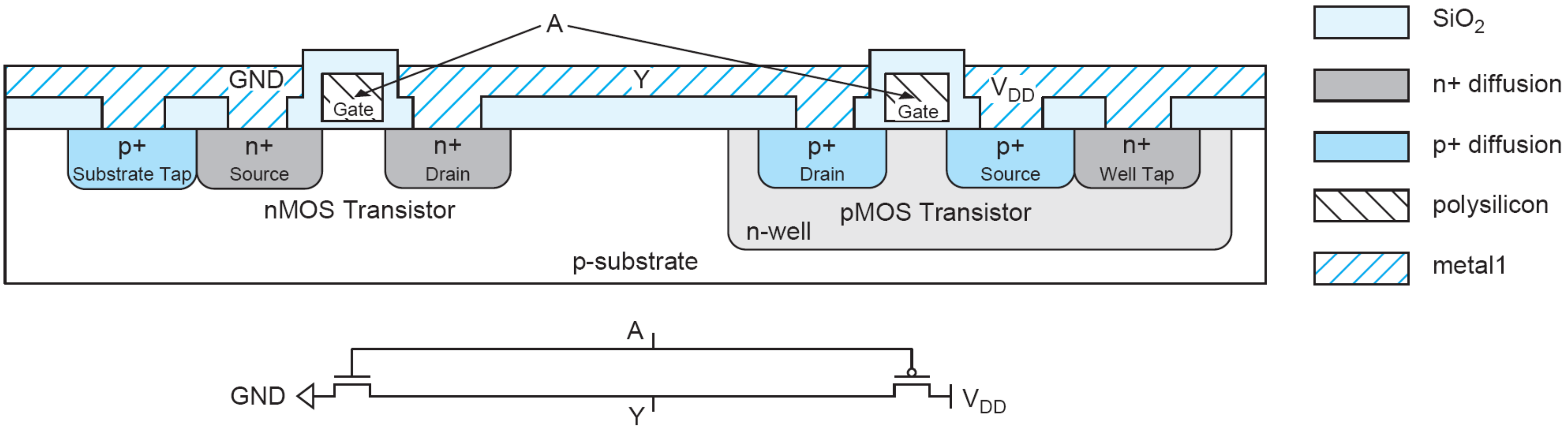


FIGURE 1.34 Inverter cross-section with well and substrate contacts. Color version on inside front cover.

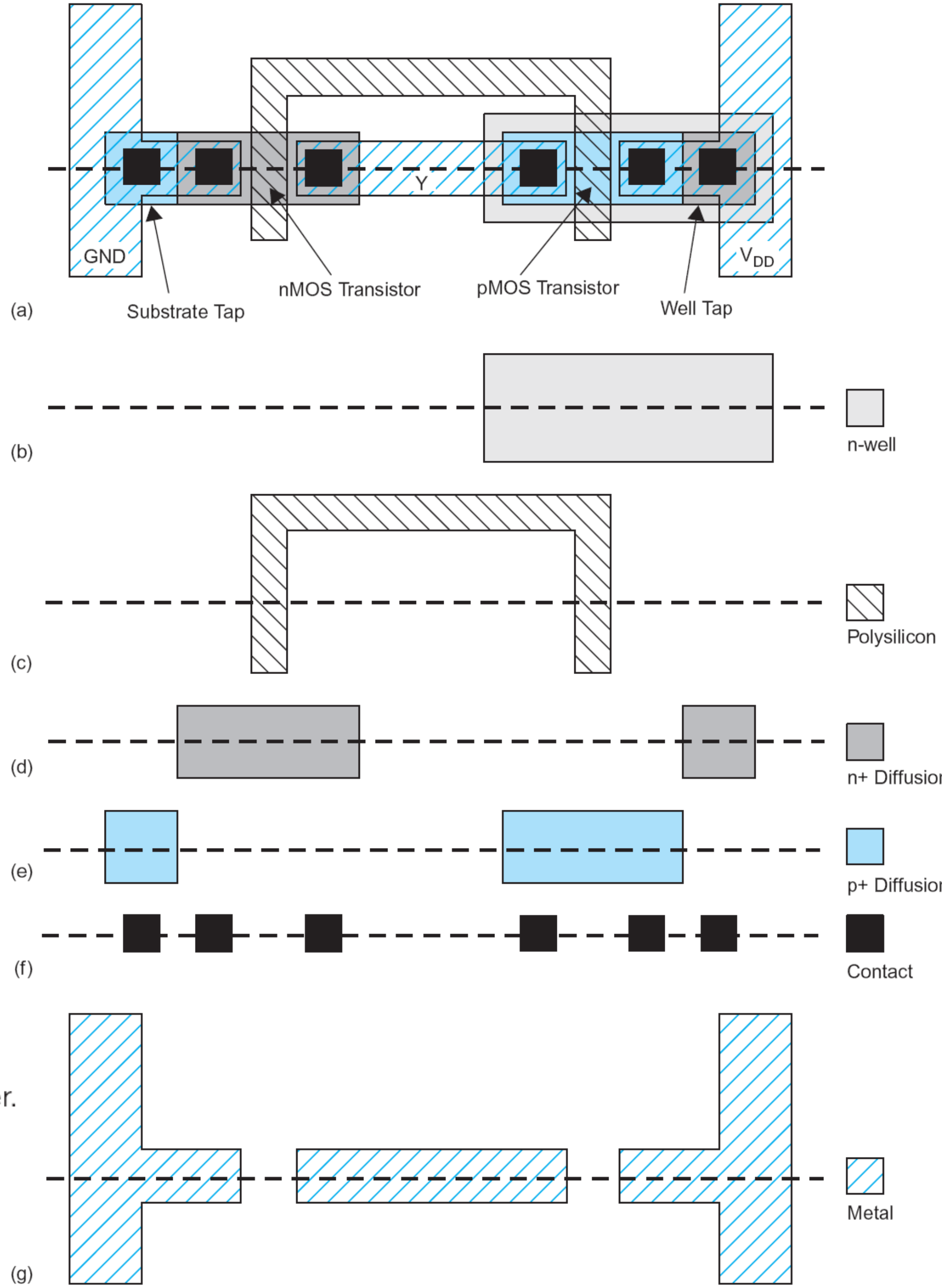


FIGURE 1.35 Inverter mask set. Color version on inside front cover.

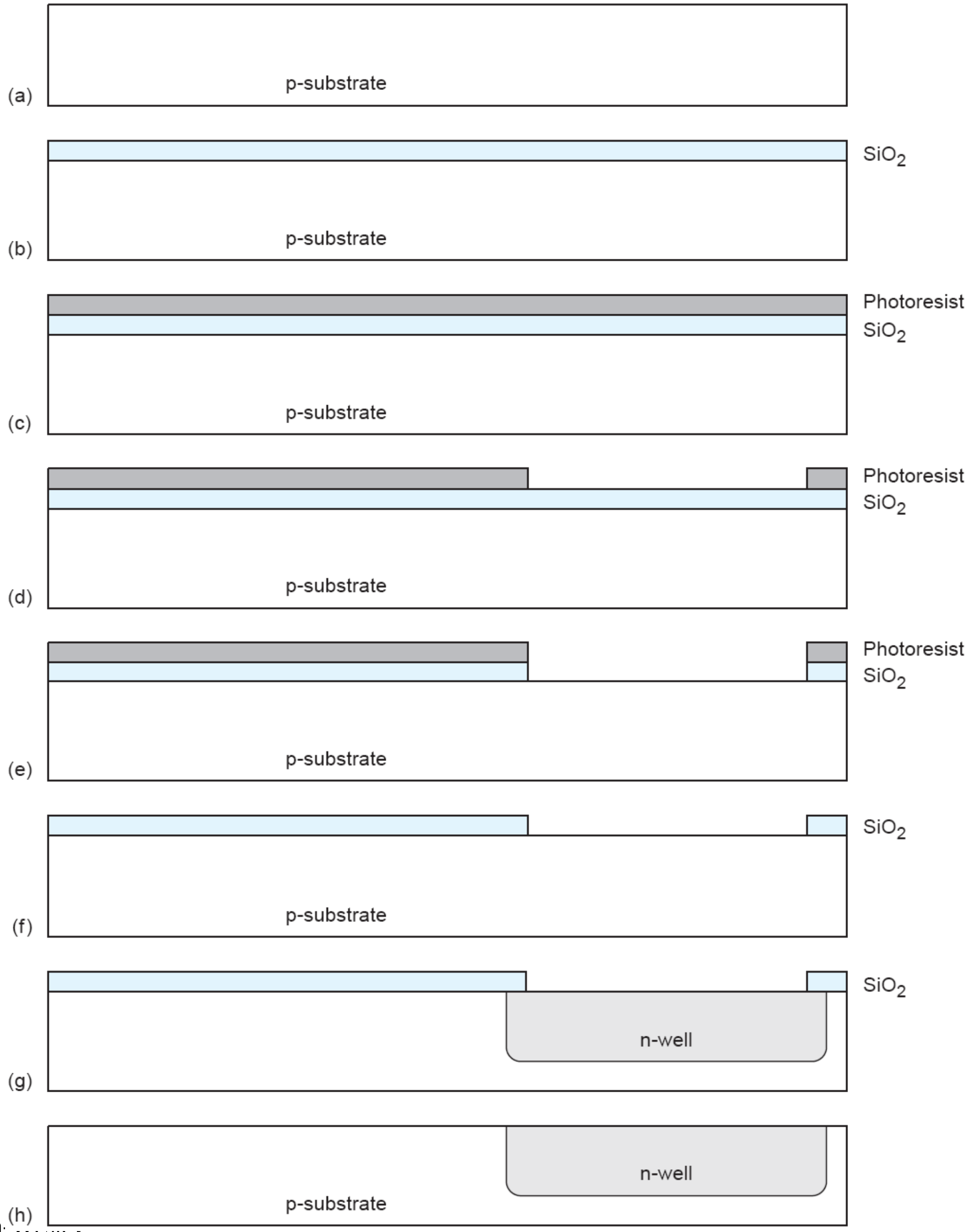


FIGURE 1.36 Cross-sections while manufacturing the n-well

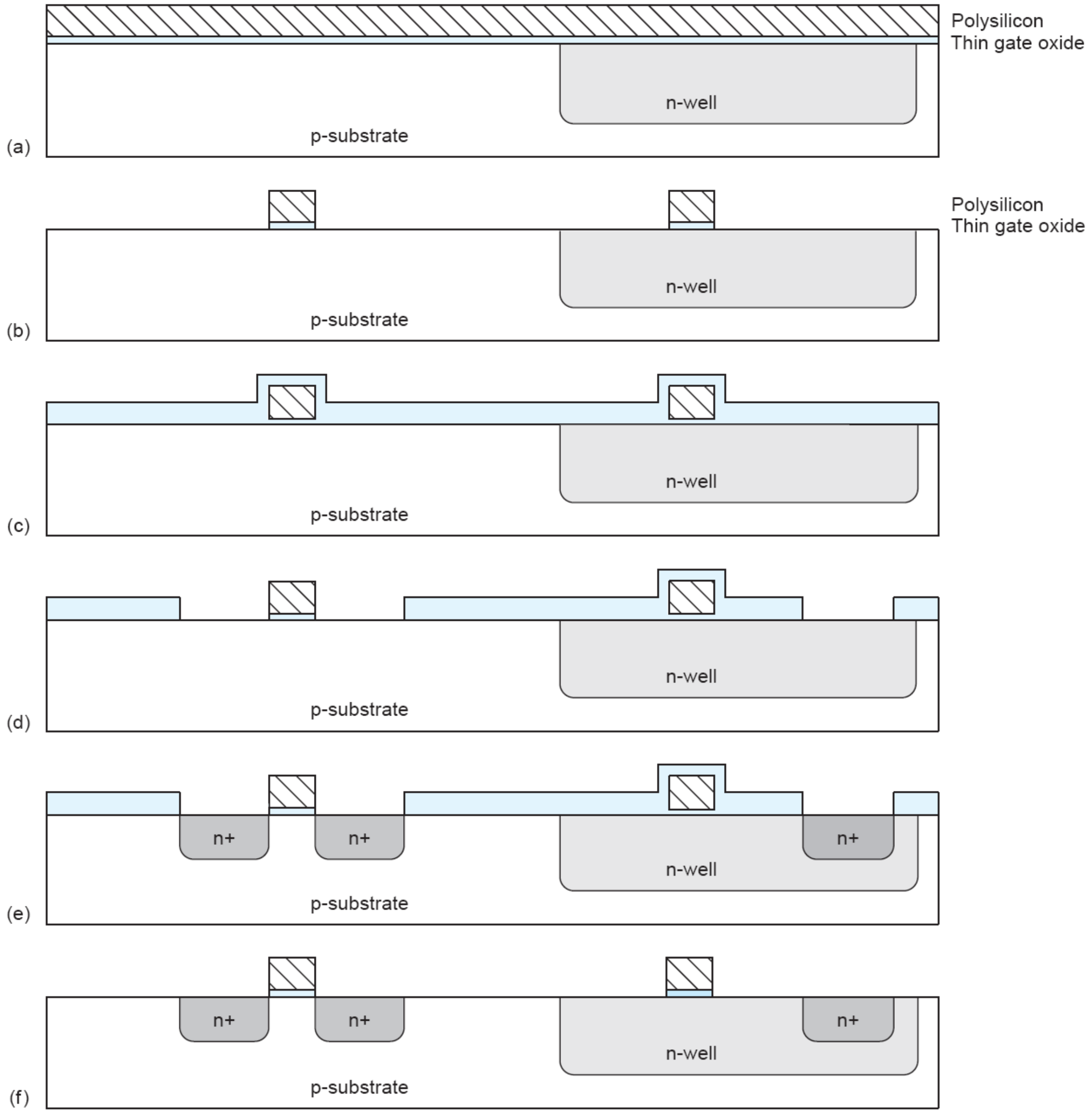


FIGURE 1.37
Cross-sections while manufactuing polysilicon and n-diffusion

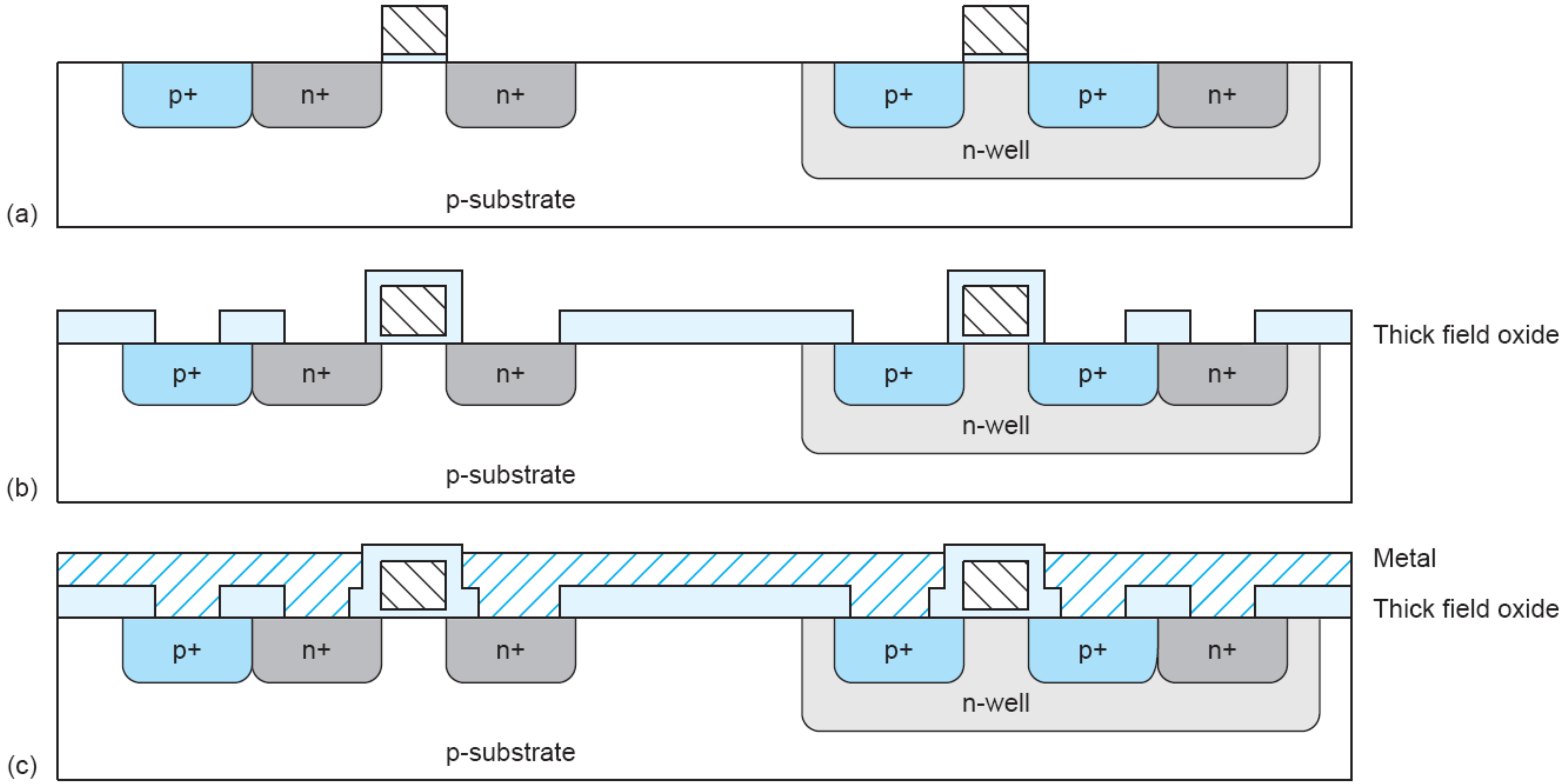


FIGURE 1.38 Cross-sections while manufacturing p-diffusion, contacts, and metal

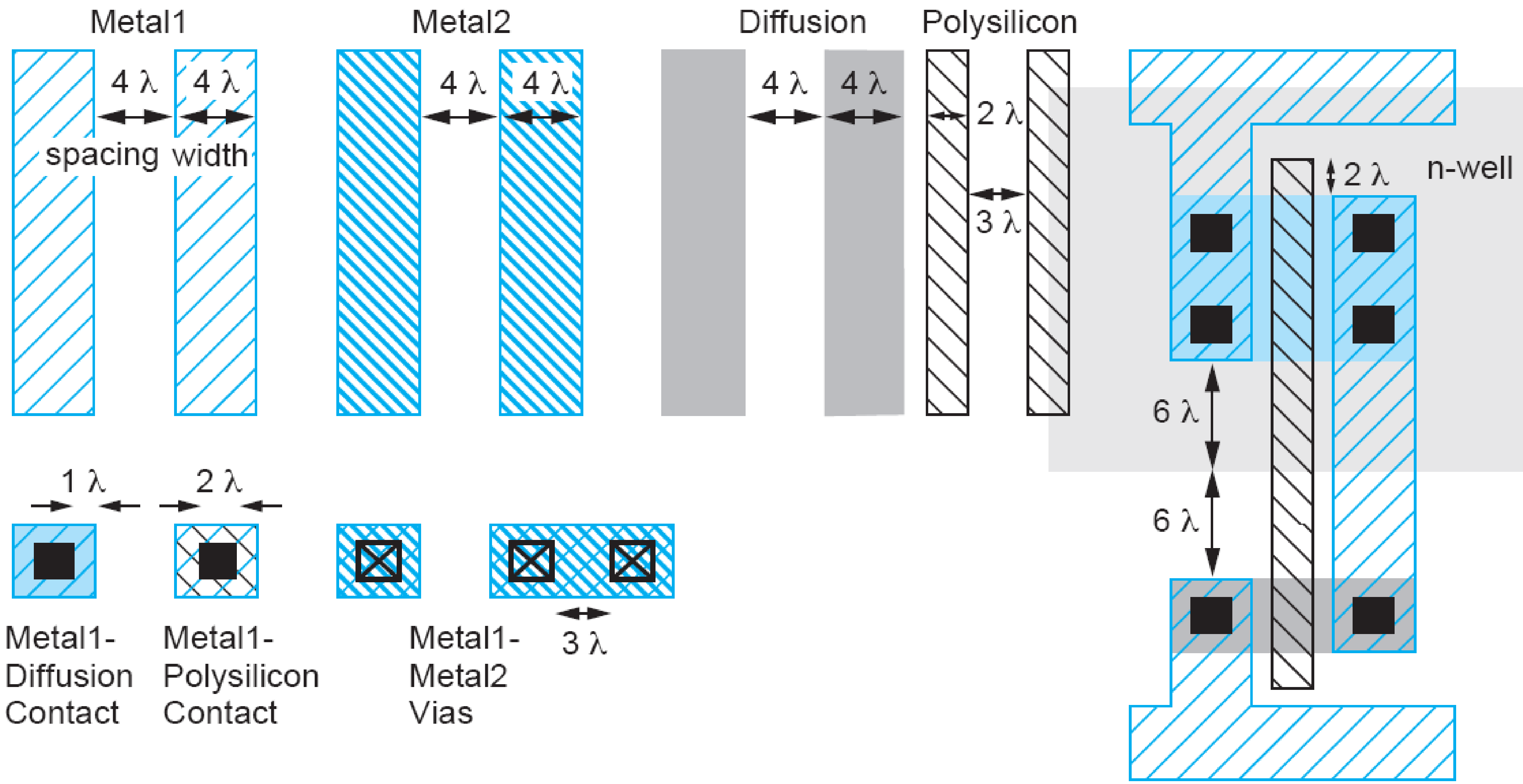


FIGURE 1.39 Simplified λ-based design rules

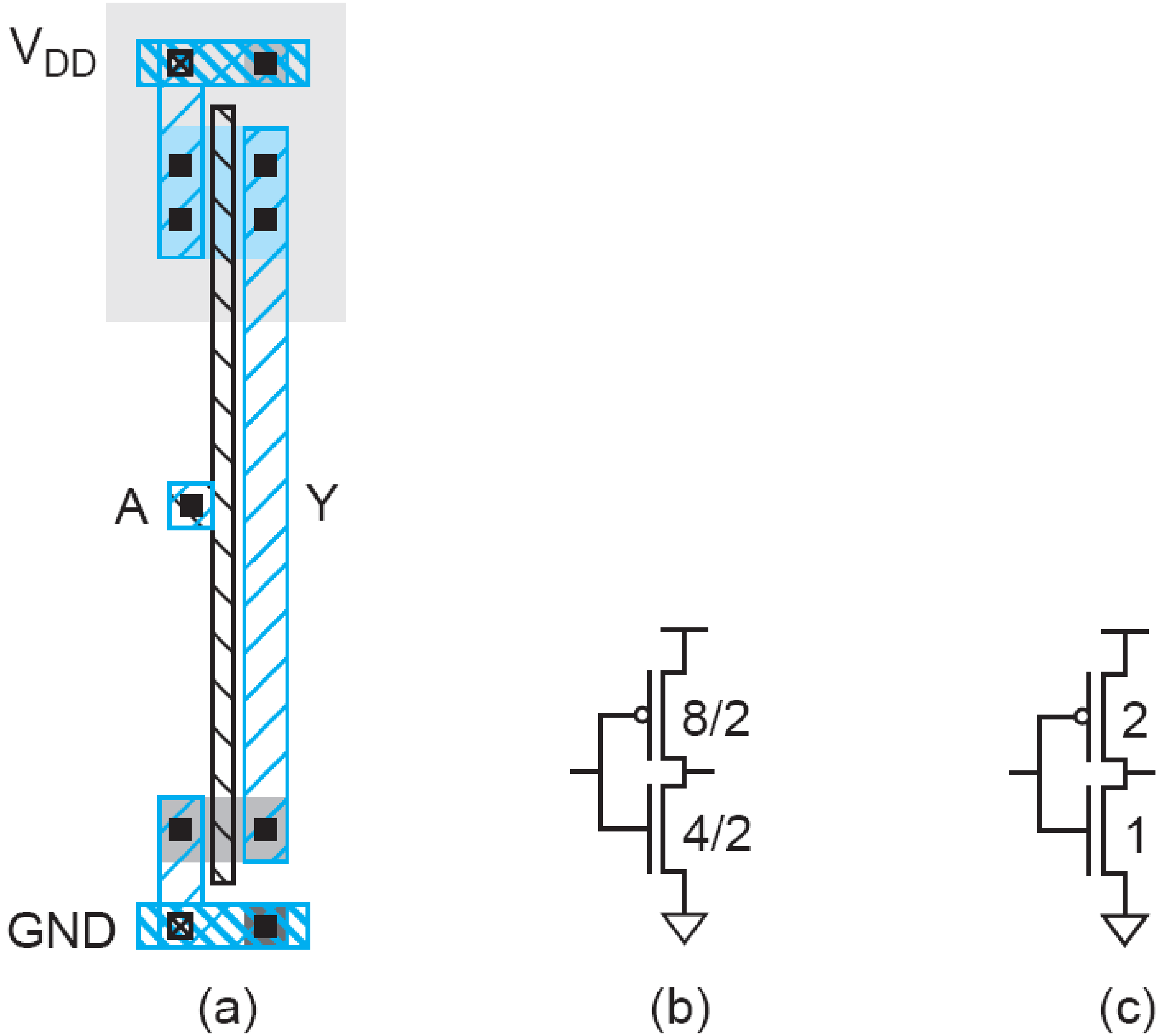


FIGURE 1.40 Inverter with dimensions labeled

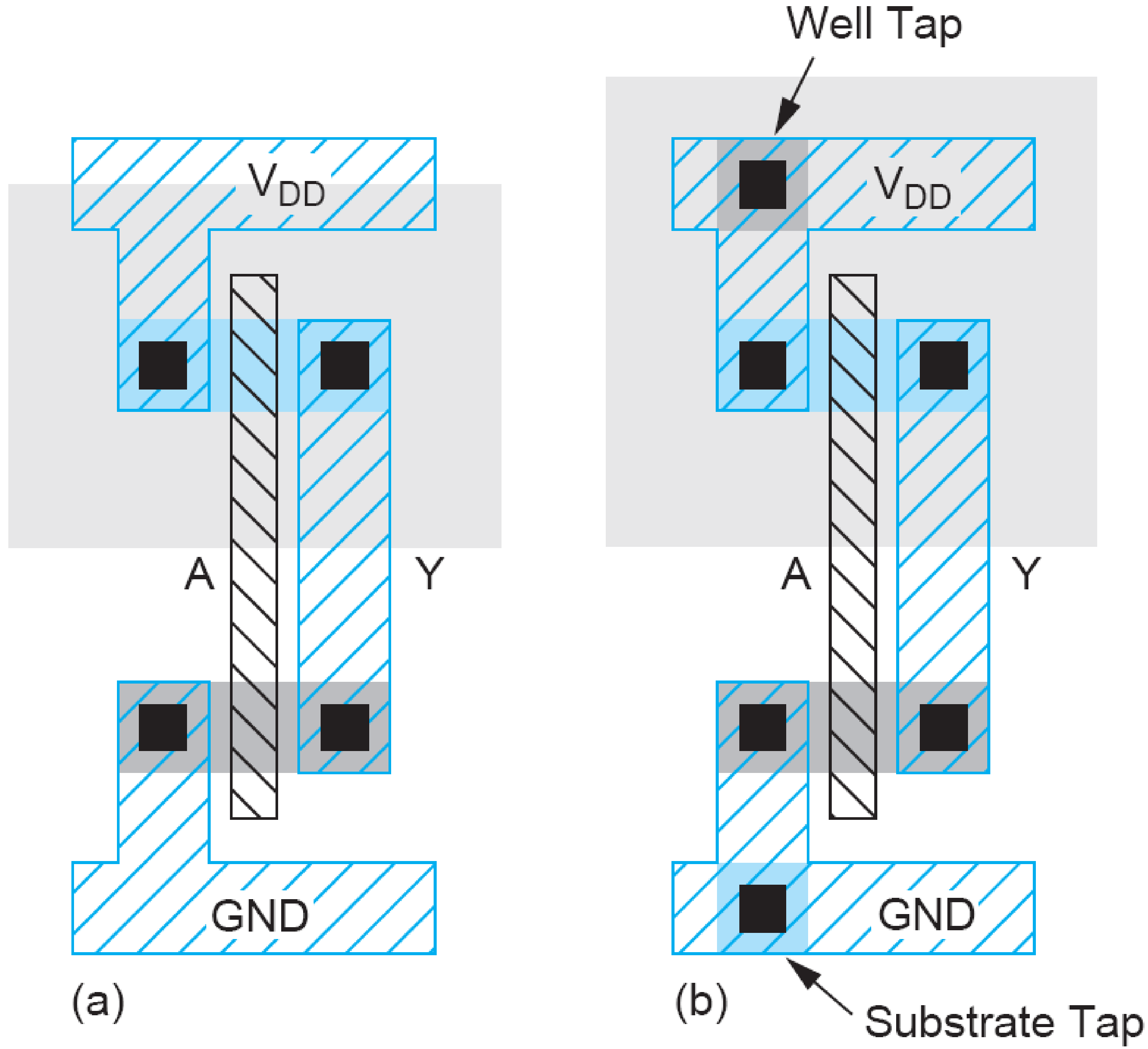


FIGURE 1.41 Inverter cell layout

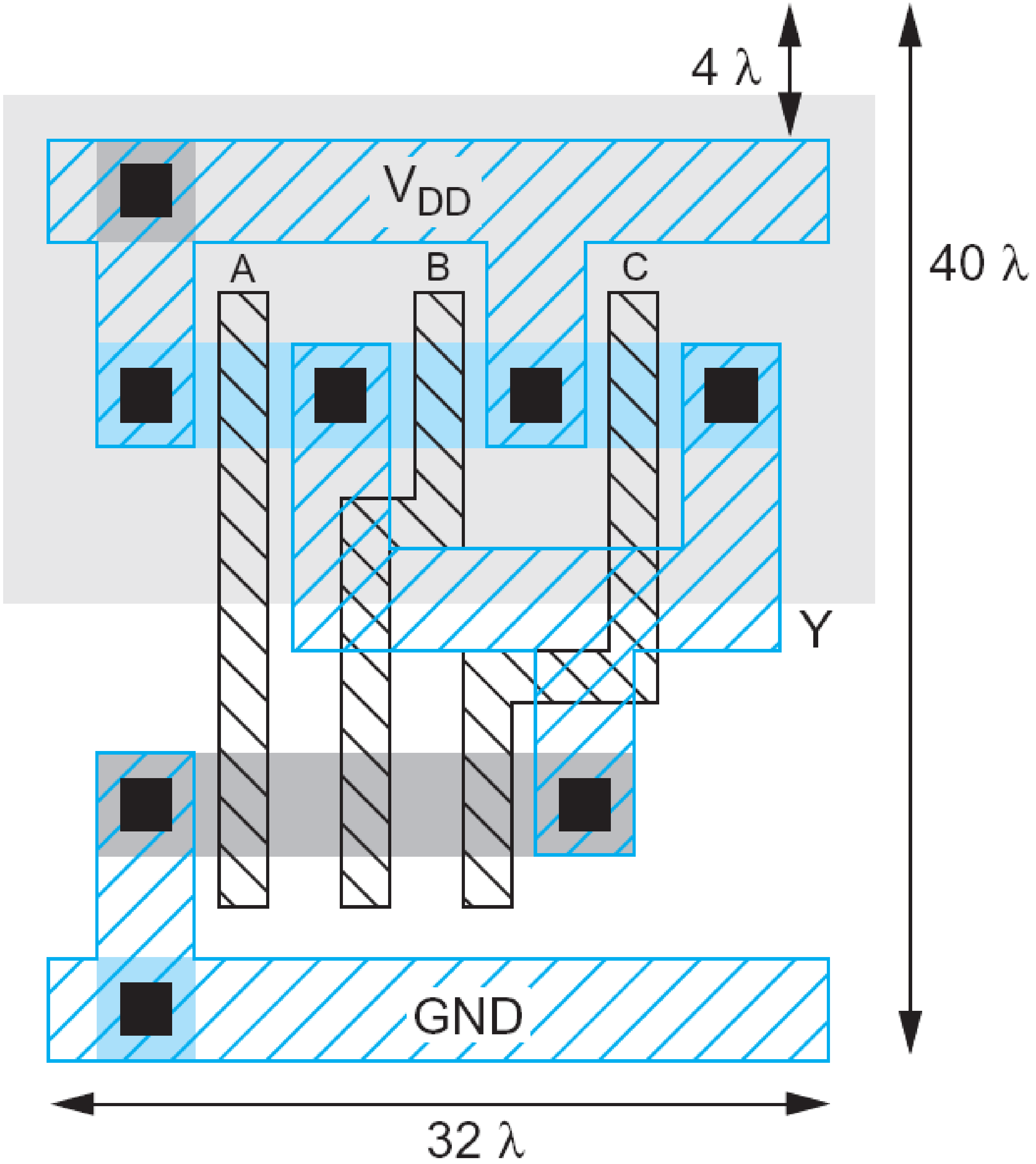


FIGURE 1.42 3-input NAND standard cell gate layouts

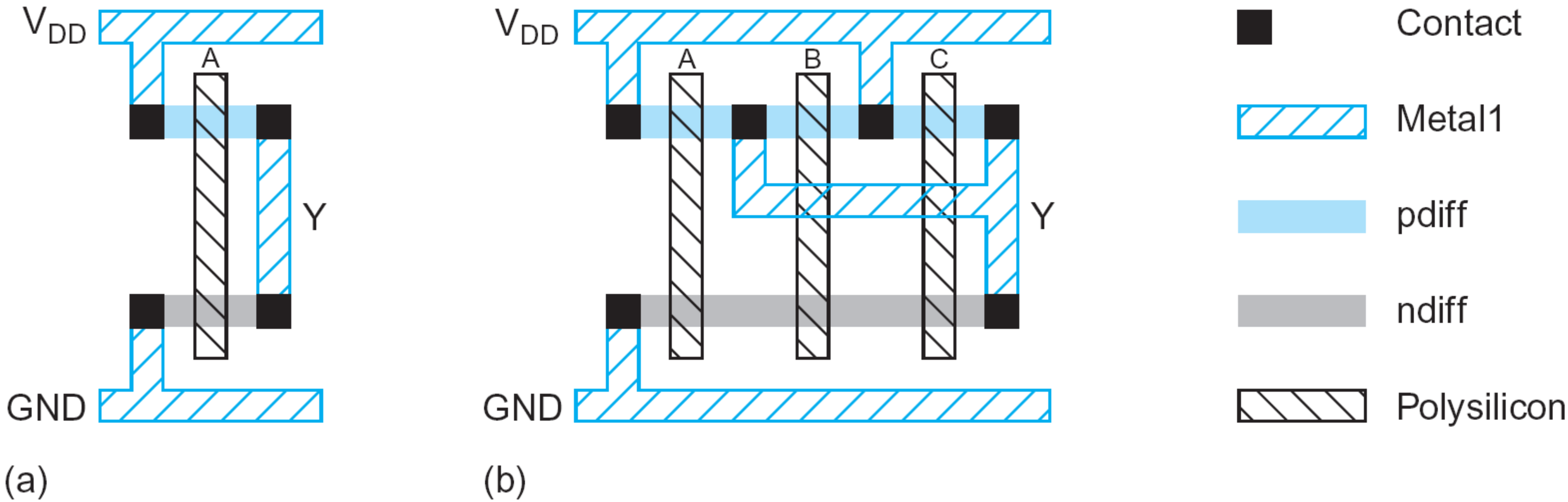


FIGURE 1.43 Stick diagrams of inverter and 3-input NAND gate. Color version on inside front cover.

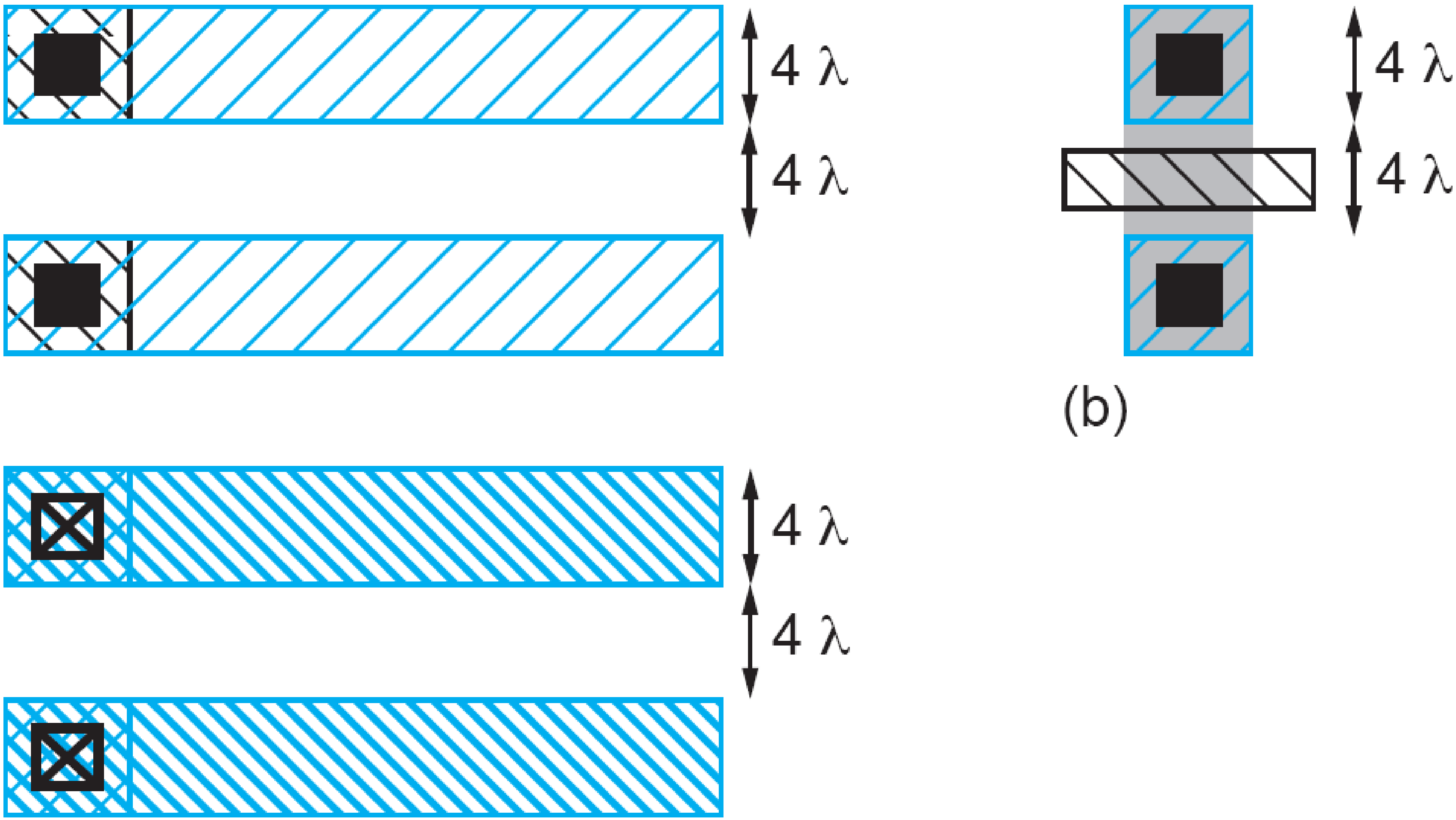
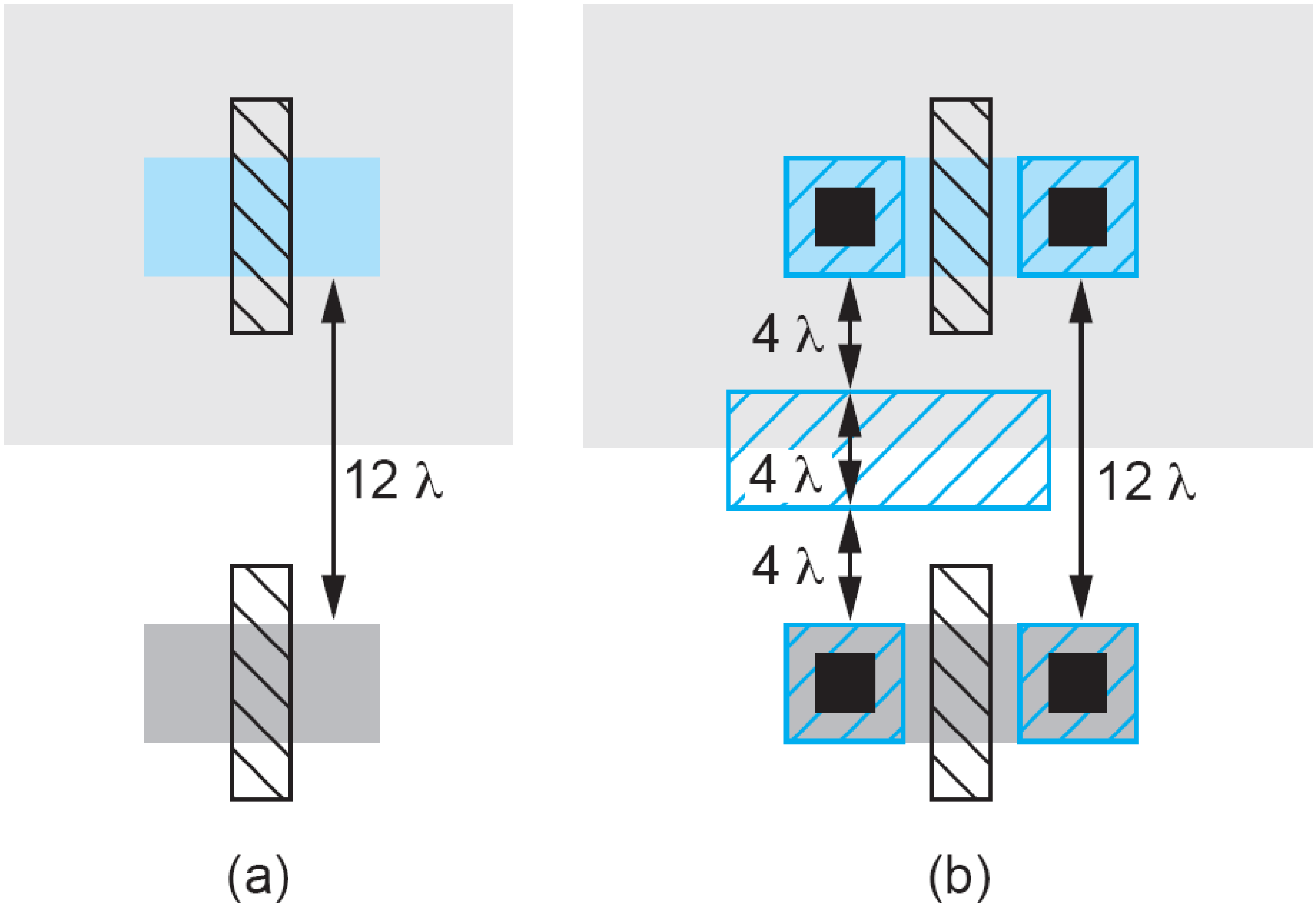


FIGURE 1.44 Pitch of routing tracks

FIGURE 1.45 Spacing between nMOS and pMOS transistors



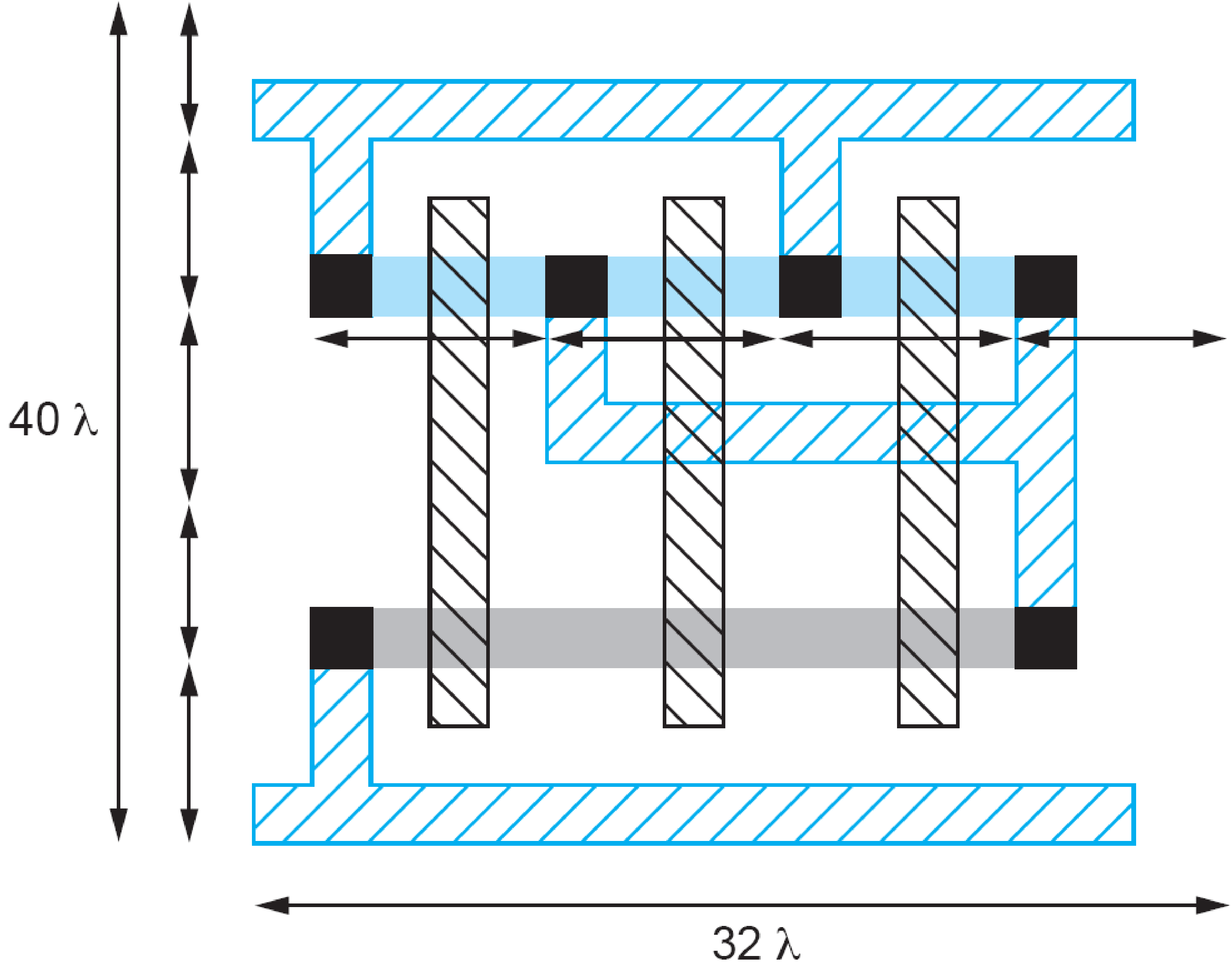


FIGURE 1.46 3-input NAND gate area estimation

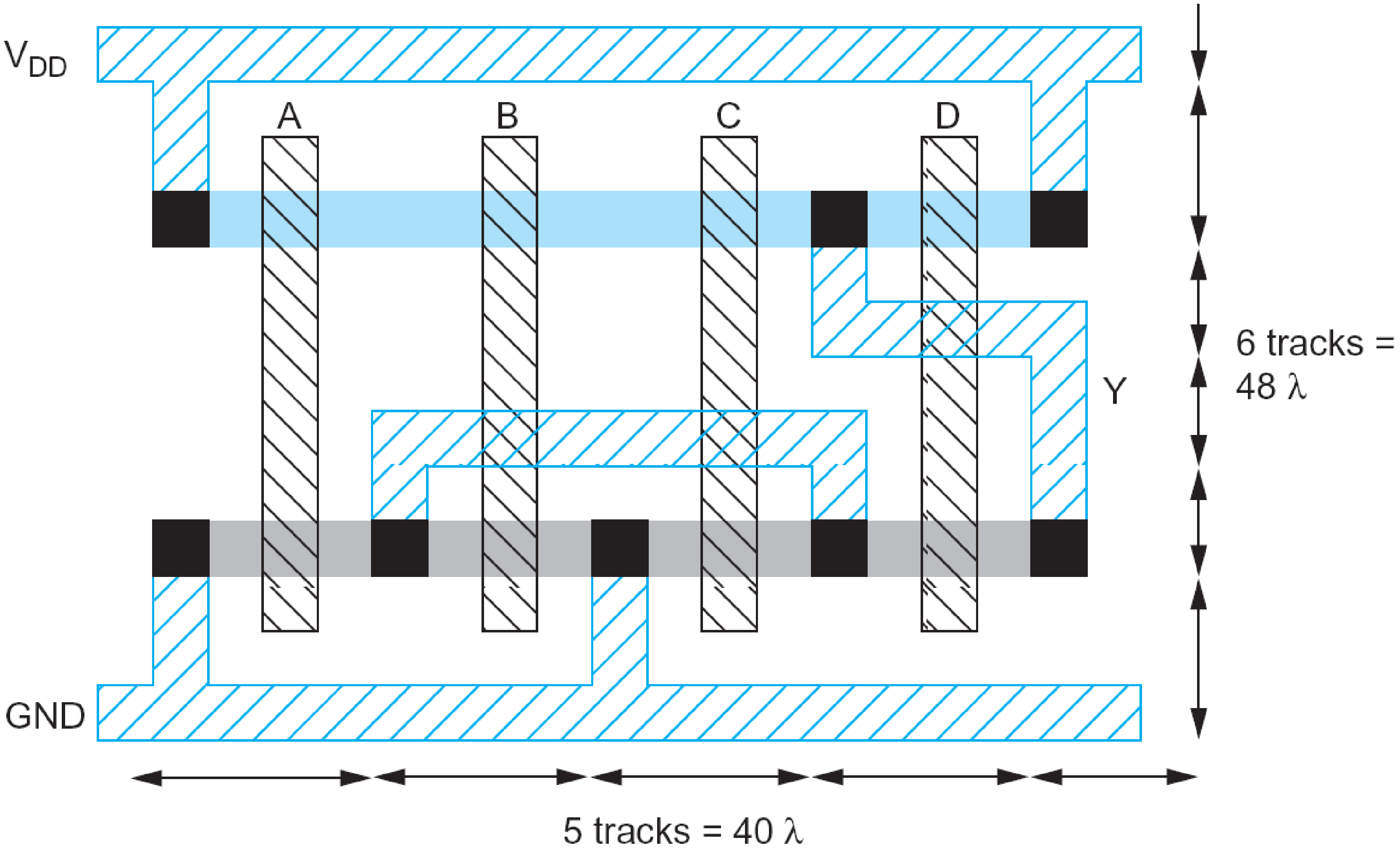
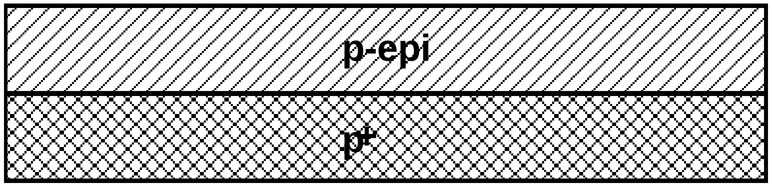
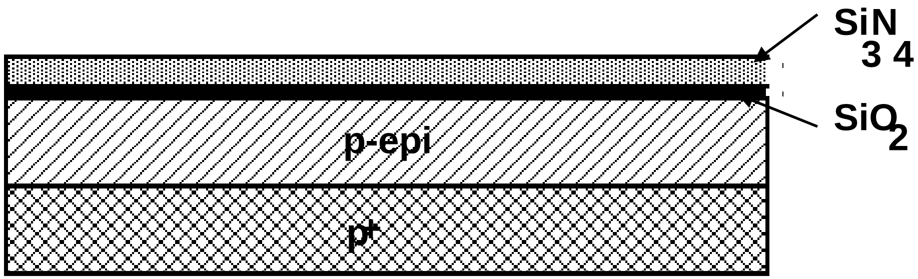


FIGURE 1.47 CMOS compound gate for function $Y = \overline{(A + B + C) \bullet D}$

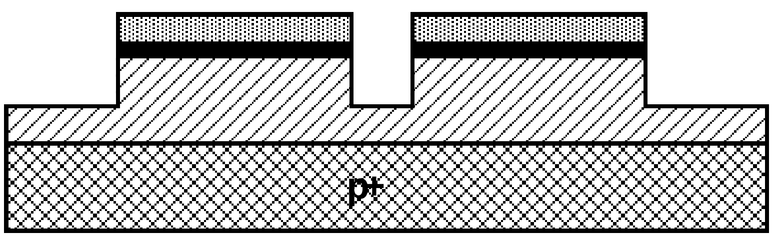
CMOS Process Walk-Through



(a) Base material: p+ substrate with p-epi layer

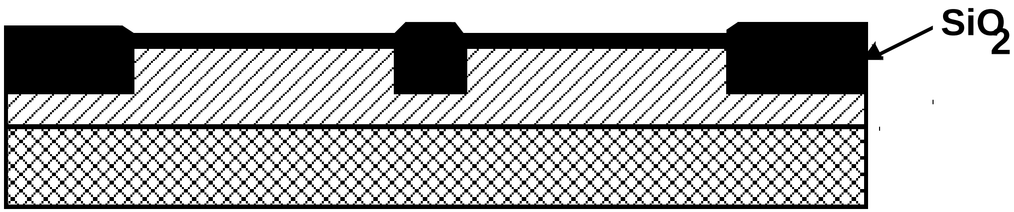


(b) After deposition of gate-oxide and sacrificial nitride (acts as a buffer layer)

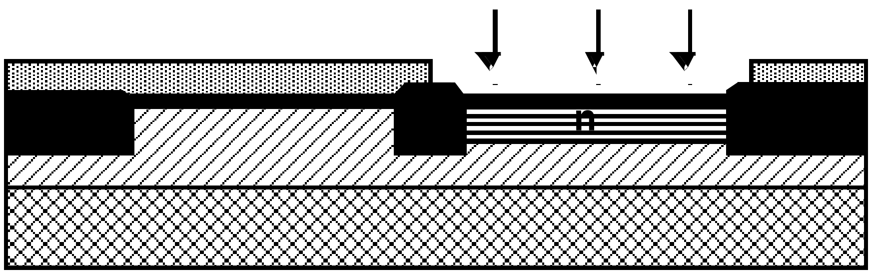


(c) After plasma etch of insulating trenches using the inverse of the active area mask

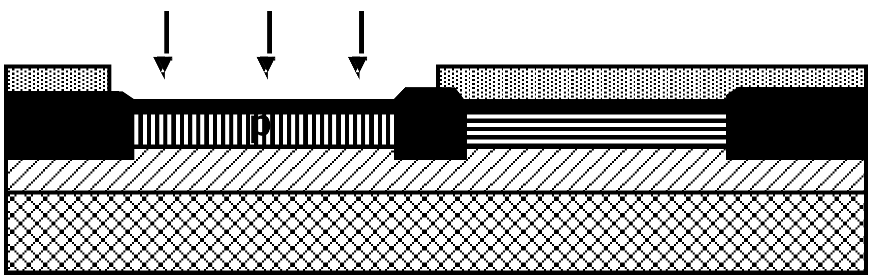
CMOS Process Walk-Through



(d) After trench filling, CMP planarization, and removal of sacrificial nitride

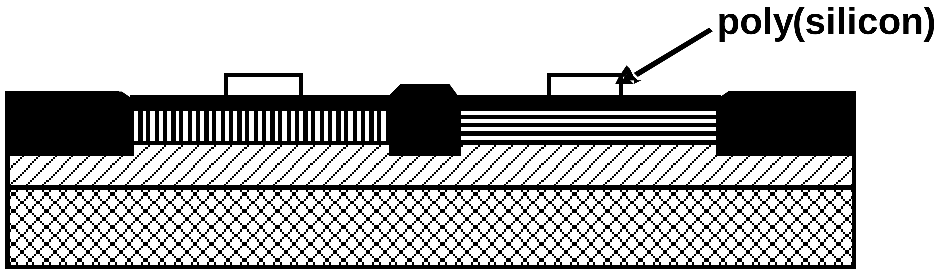


(e) After n-well and V_{Tp} adjust implants

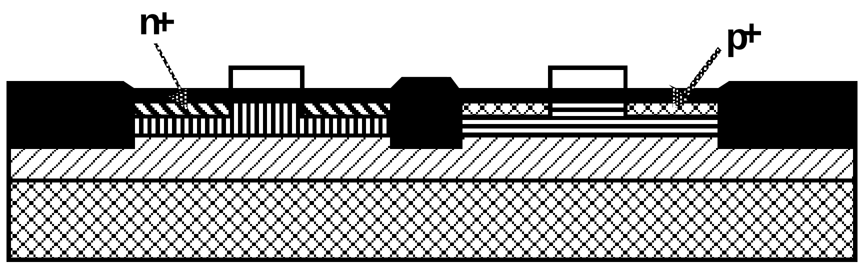


(f) After p-well and V_{Tn} adjust implants

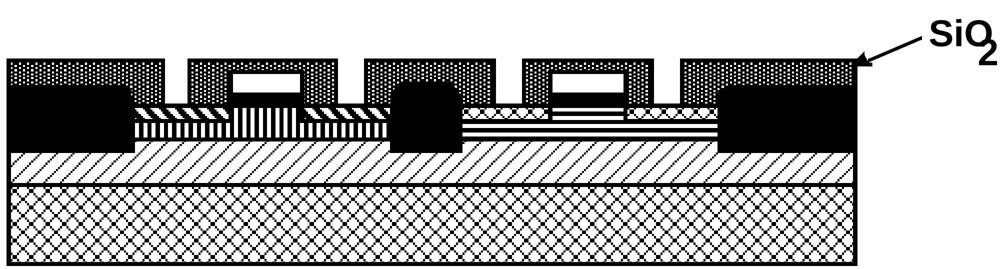
CMOS Process Walk-Through



(g) After polysilicon deposition and etch

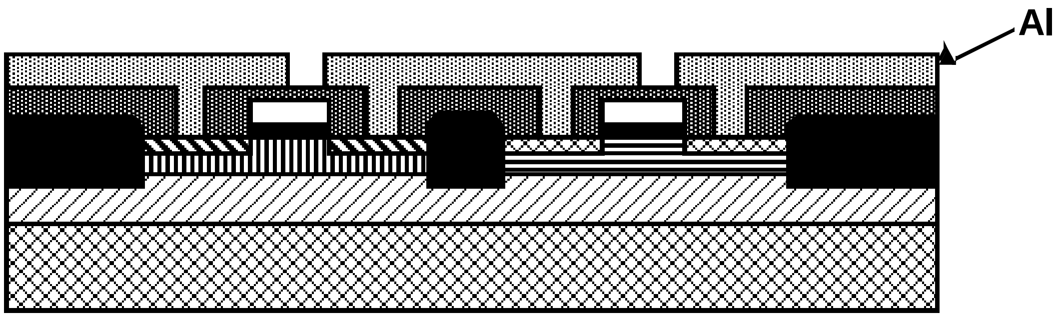


(h) After n+ source/drain and p+ source/drain implants. These steps also dope the polysilicon.

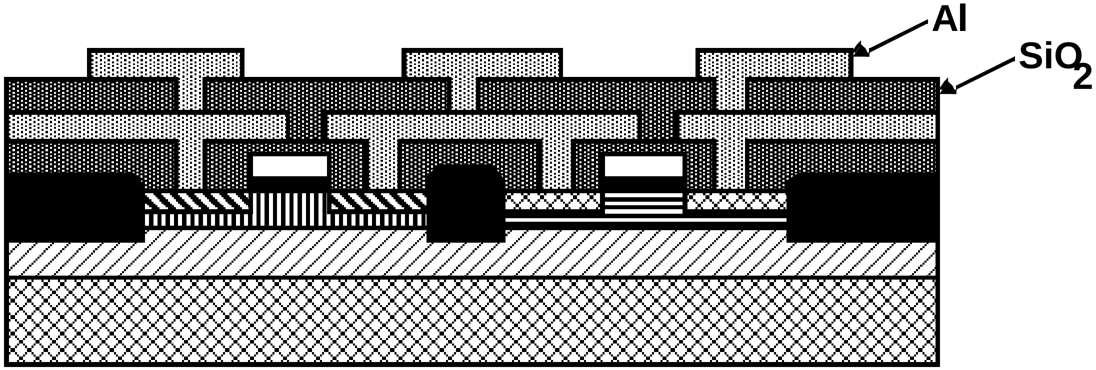


(i) After deposition of SiO_2 insulator and contact hole etch.

CMOS Process Walk-Through

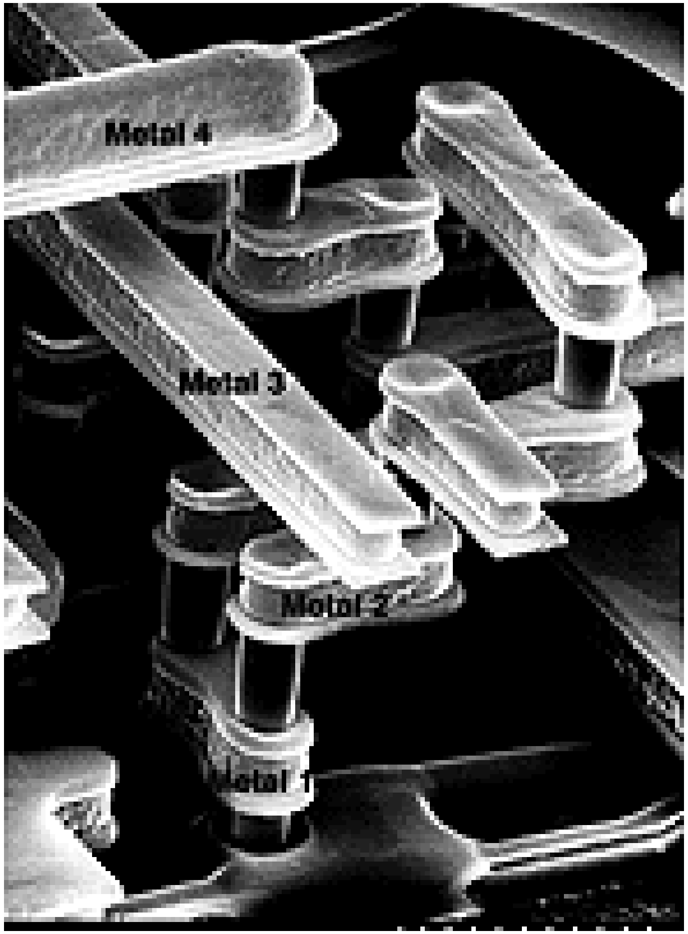


(j) After deposition and patterning of first Al layer.

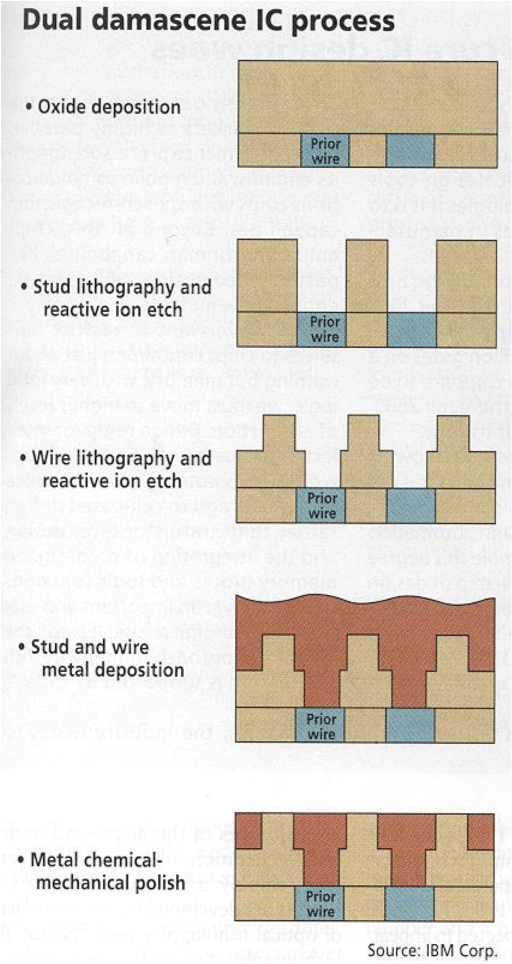


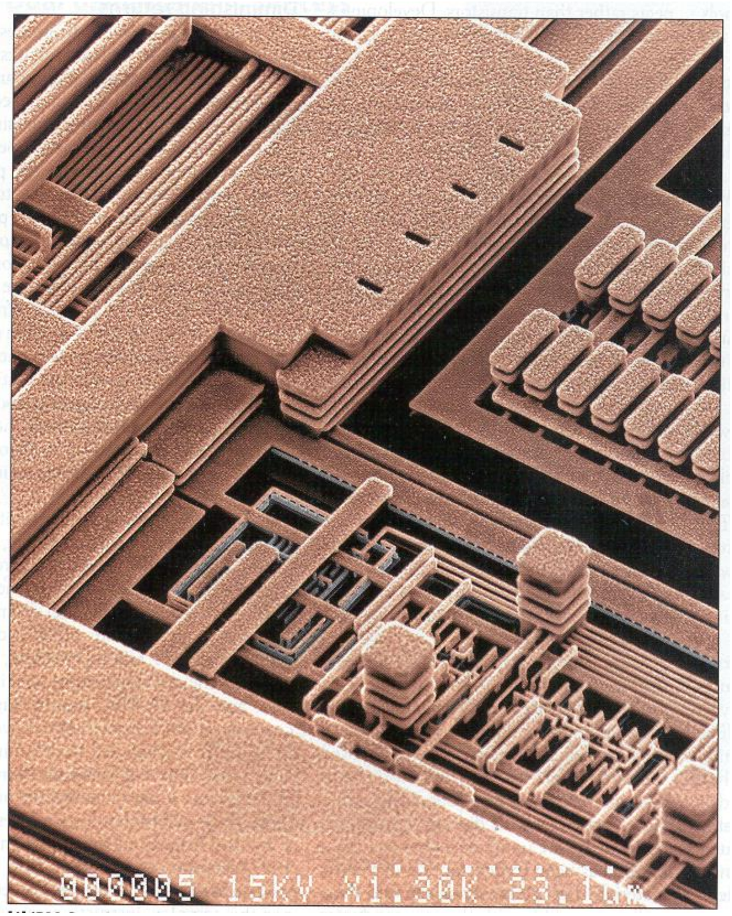
(k) After deposition of SiO_2 insulator, etching of via's, deposition and patterning of second layer of Al.

Advanced Metallization



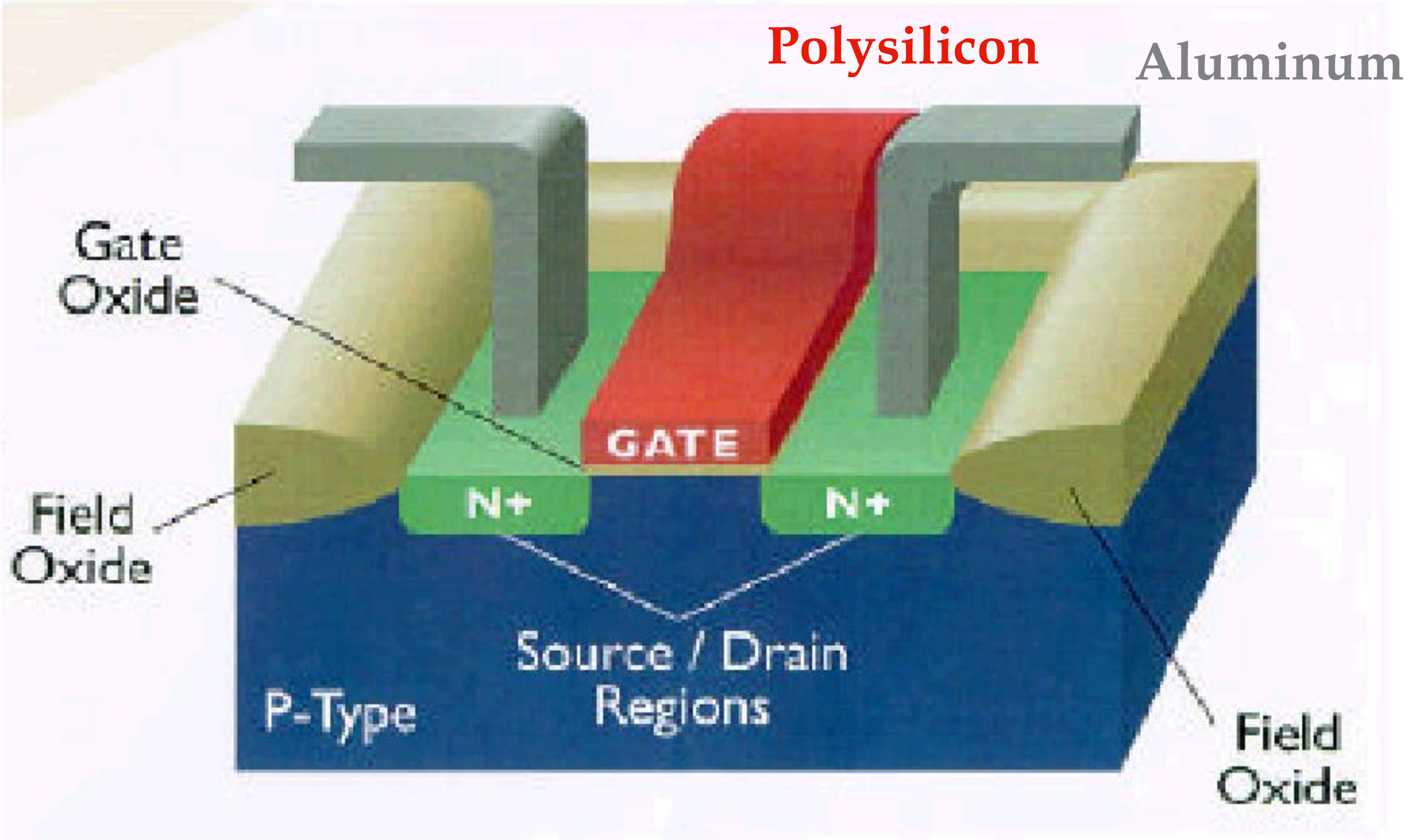
Advanced Metallization



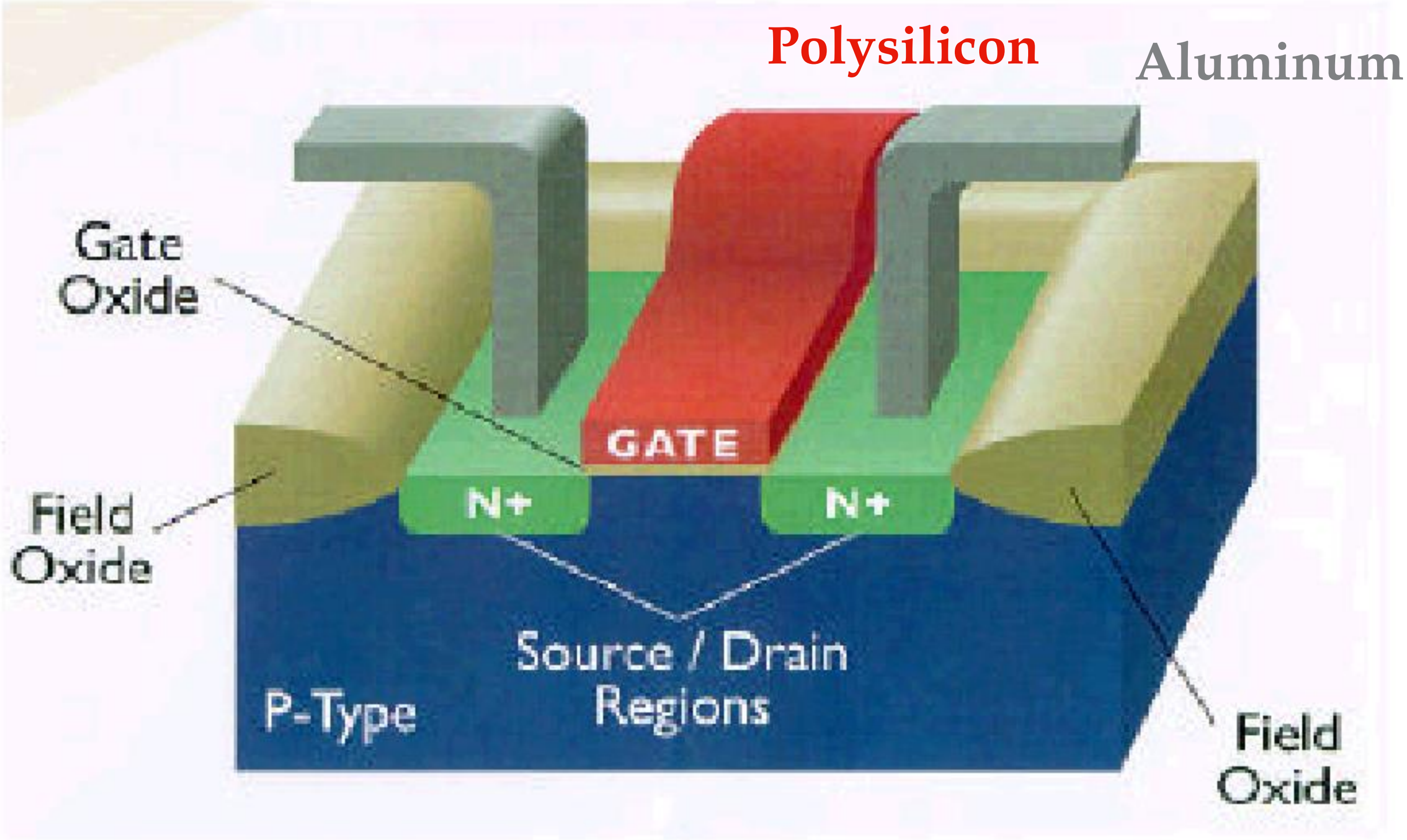


Design Rules

3D Perspective



3D Perspective



Design Rules

- Interface between designer and process engineer
- Guidelines for constructing process masks
- Unit dimension: Minimum line width
  - scalable design rules: lambda parameter
  - absolute dimensions (micron rules)

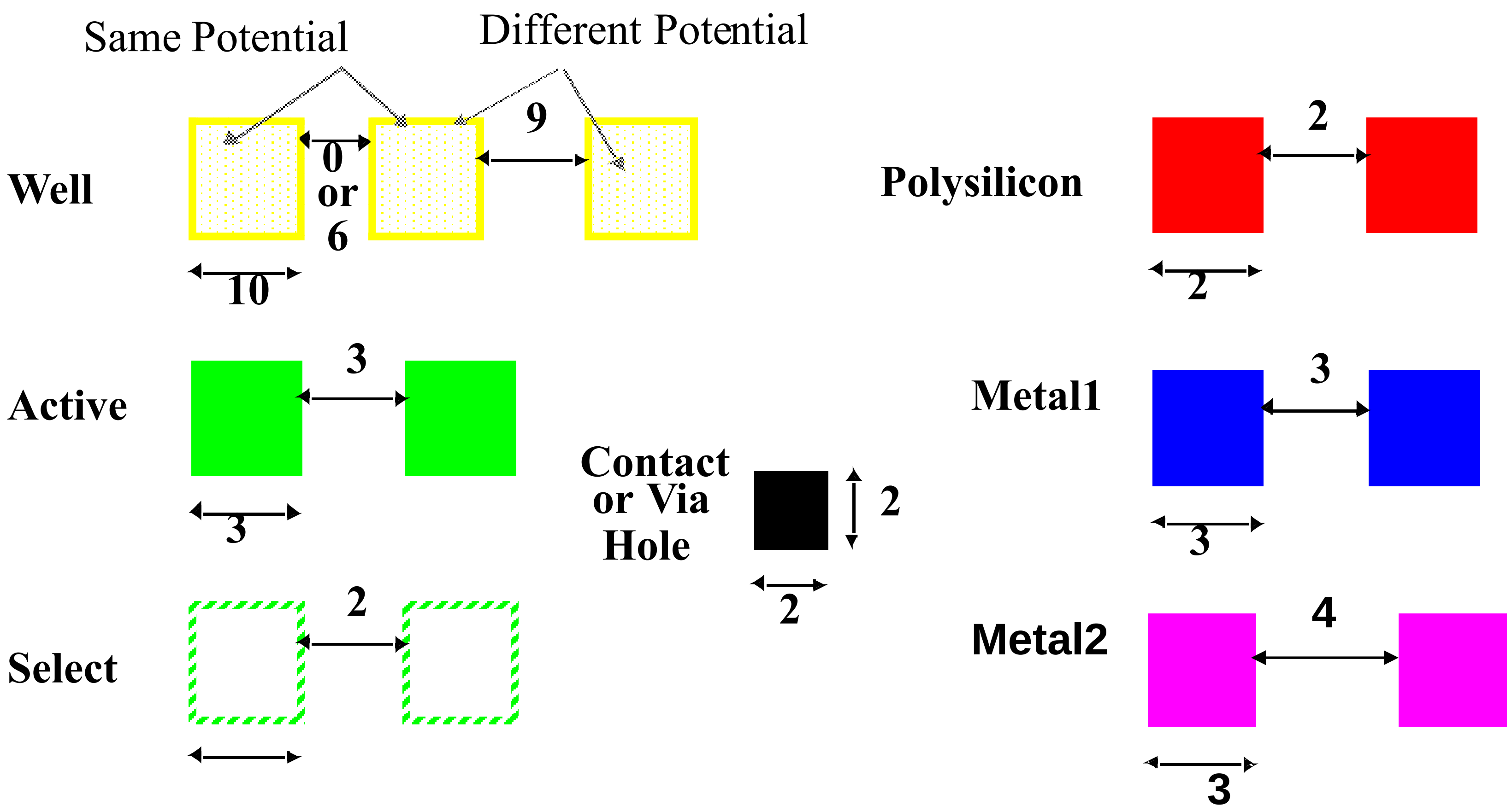
CMOS Process Layers

Layer	Color	Representation
Well (p,n)	Yellow	
Active Area (n+,p+)	Green	
Select (p+,n+)	Green	
Polysilicon	Red	
Metal1	Blue	
Metal2	Magenta	
Contact To Poly	Black	
Contact To Diffusion	Black	
Via	Black	

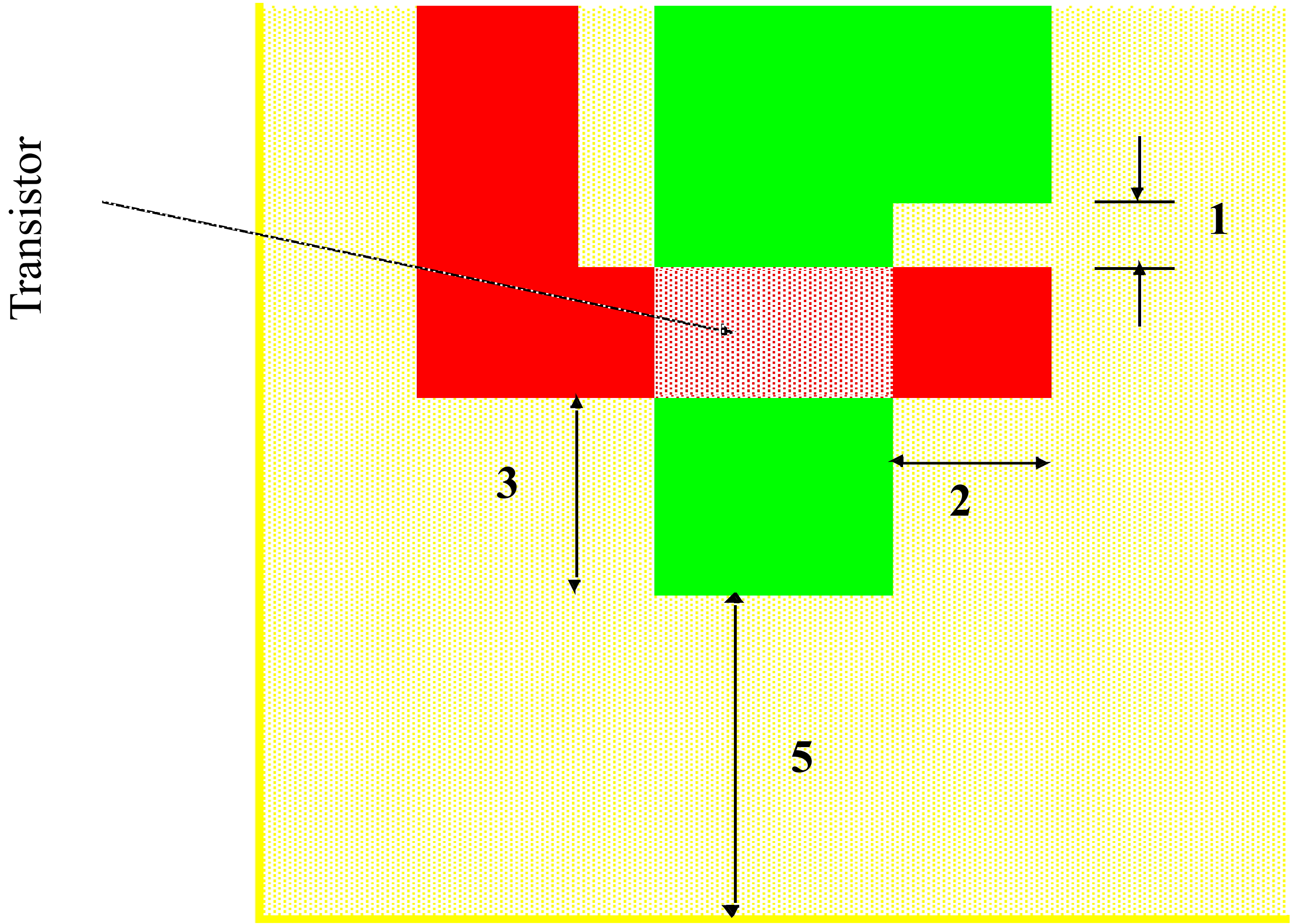
Layers in 0.25 μm CMOS process

Layer Description	Representation				
metal	m1	m2	m3	m4	m5
well	nw				
polysilicon	poly				
contacts & vias	ct	v12,v23,v34,v45	nwc	pwc	
active area and FETs	ndif	pdif	nfet	pfet	
select	nplus	pplus	prb		

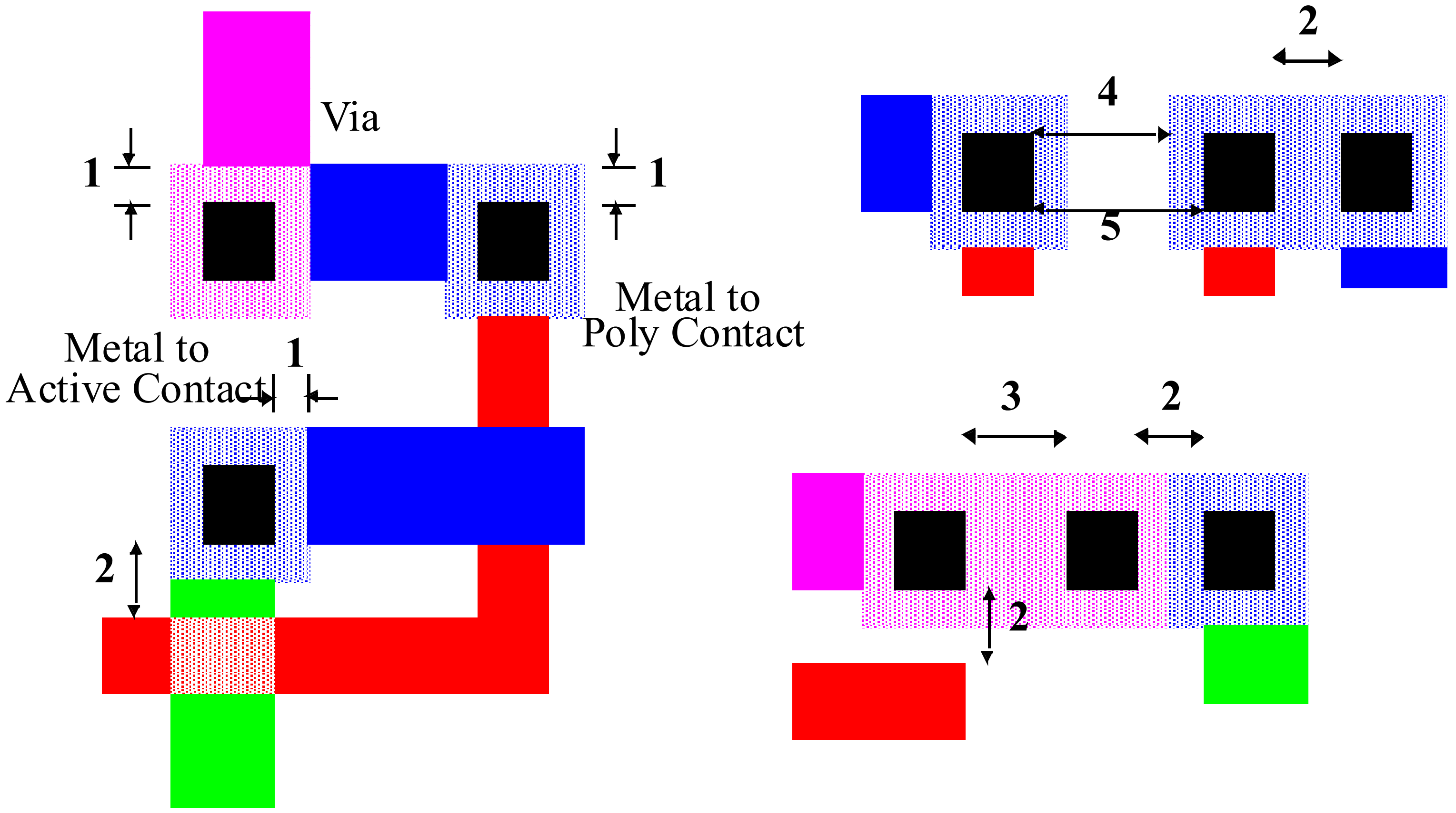
Intra-Layer Design Rules



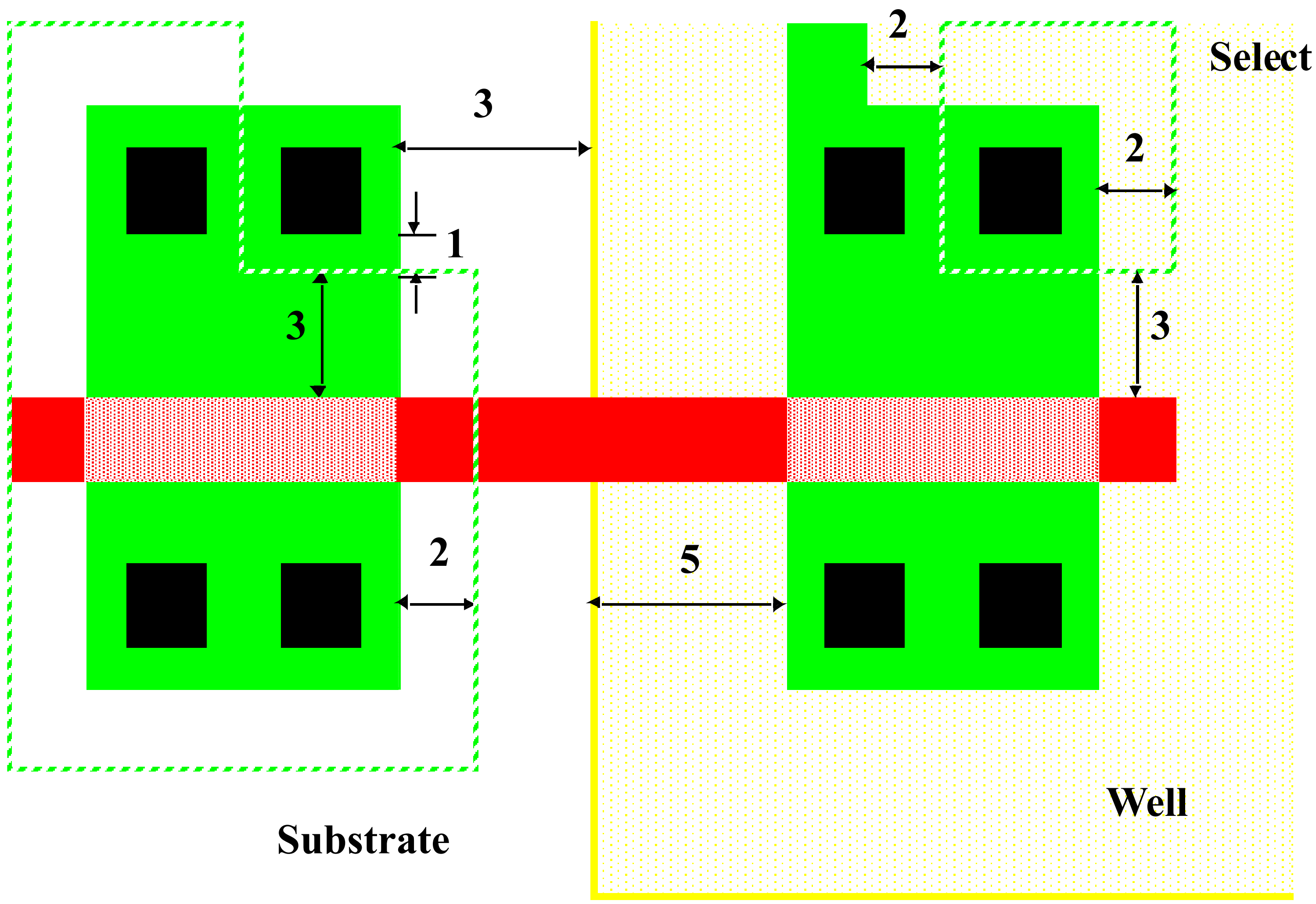
Transistor Layout



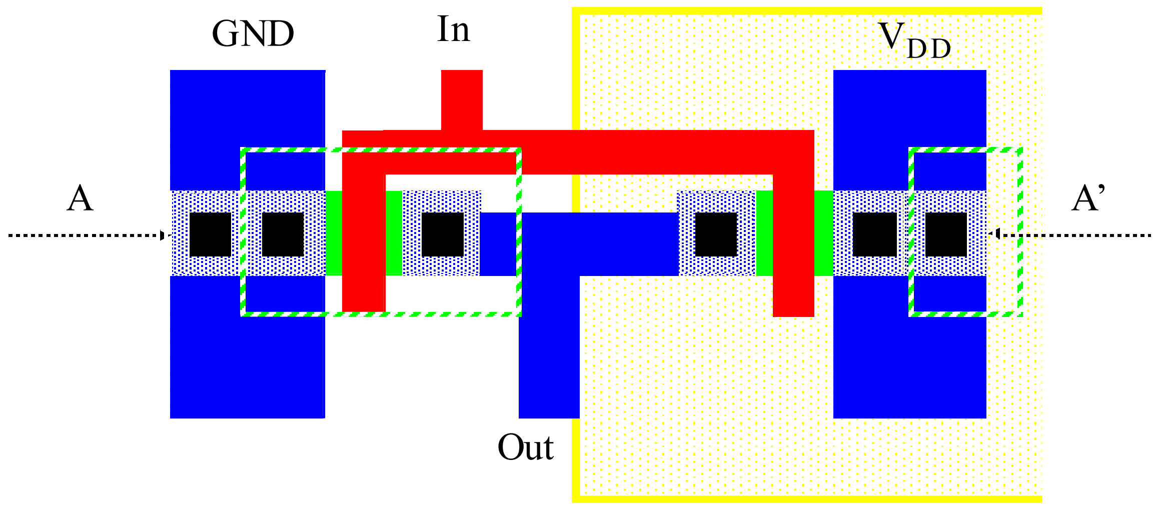
Vias and Contacts



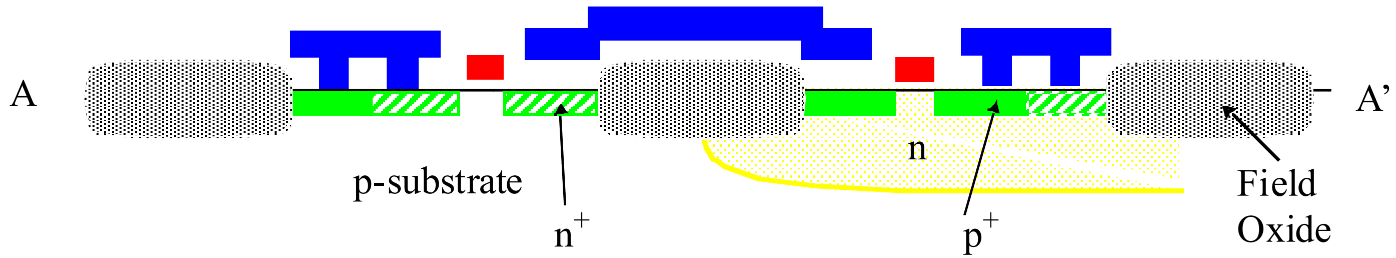
Select Layer



CMOS Inverter Layout

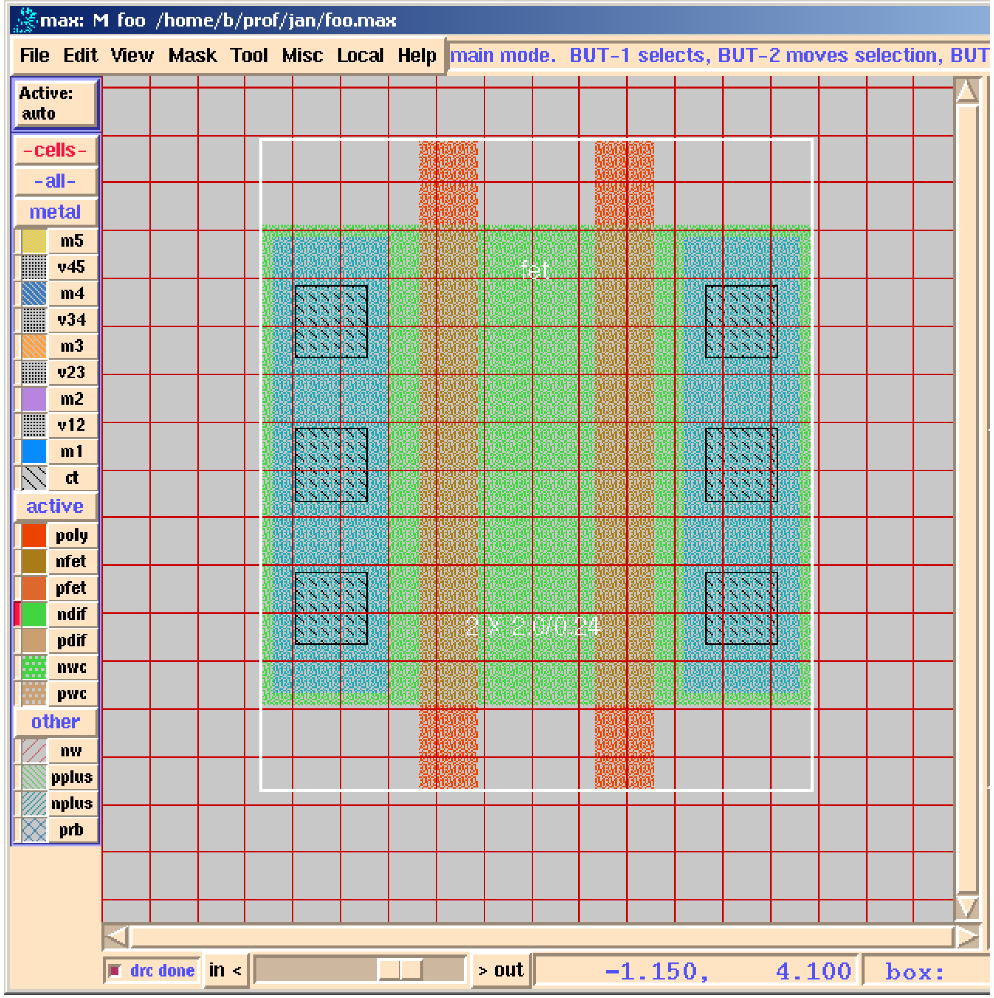


(a) Layout

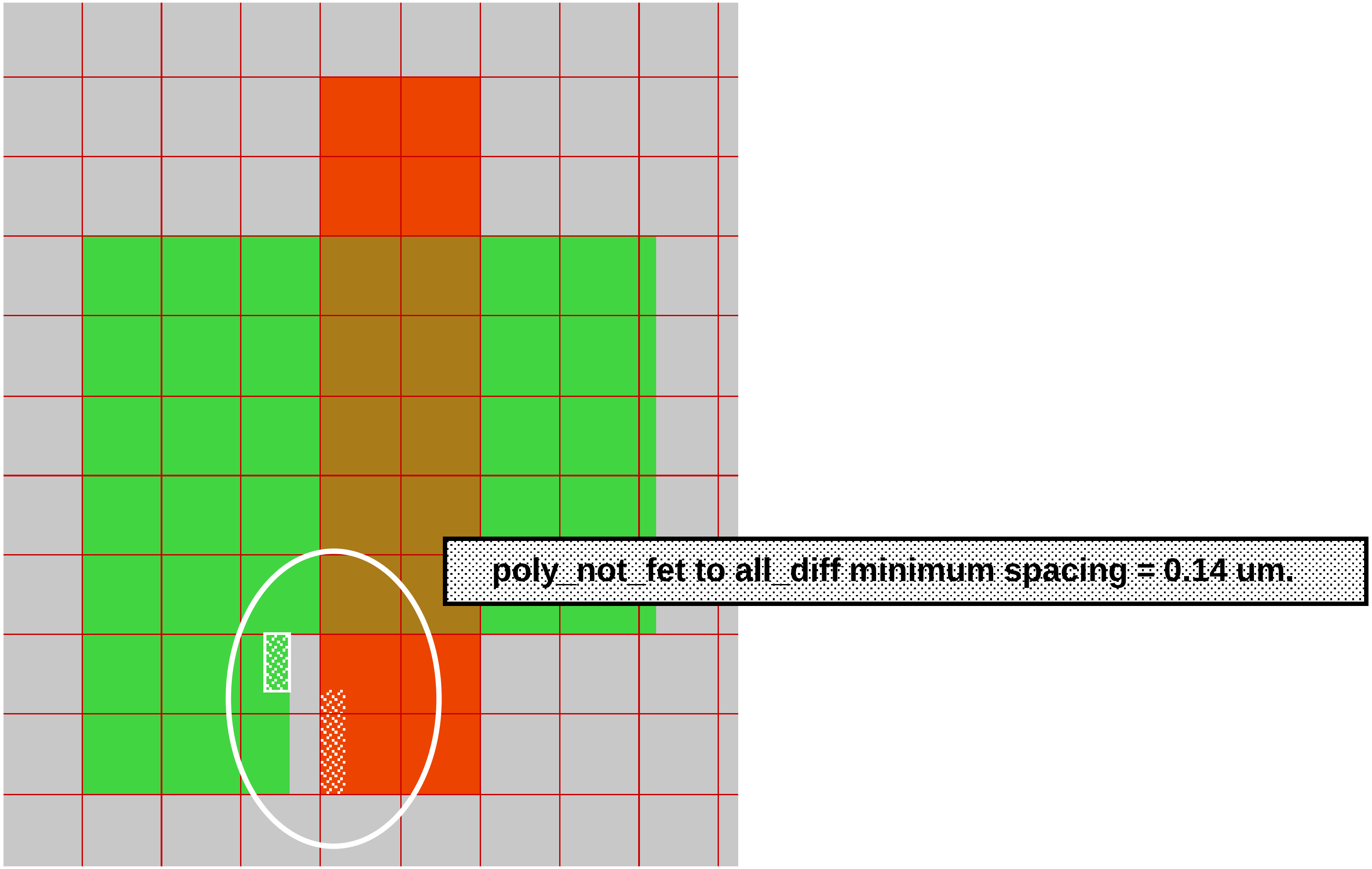


(b) Cross-Section along A-A'

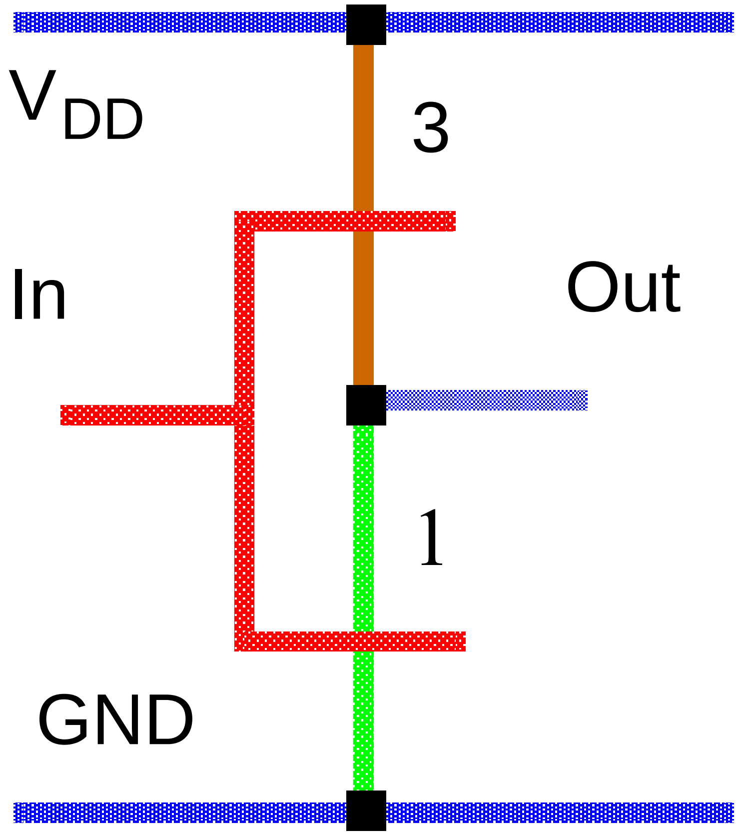
Layout Editor



Design Rule Checker



Sticks Diagram



Stick diagram of inverter

- Dimensionless layout entities
- Only topology is important
- Final layout generated by "compaction" program

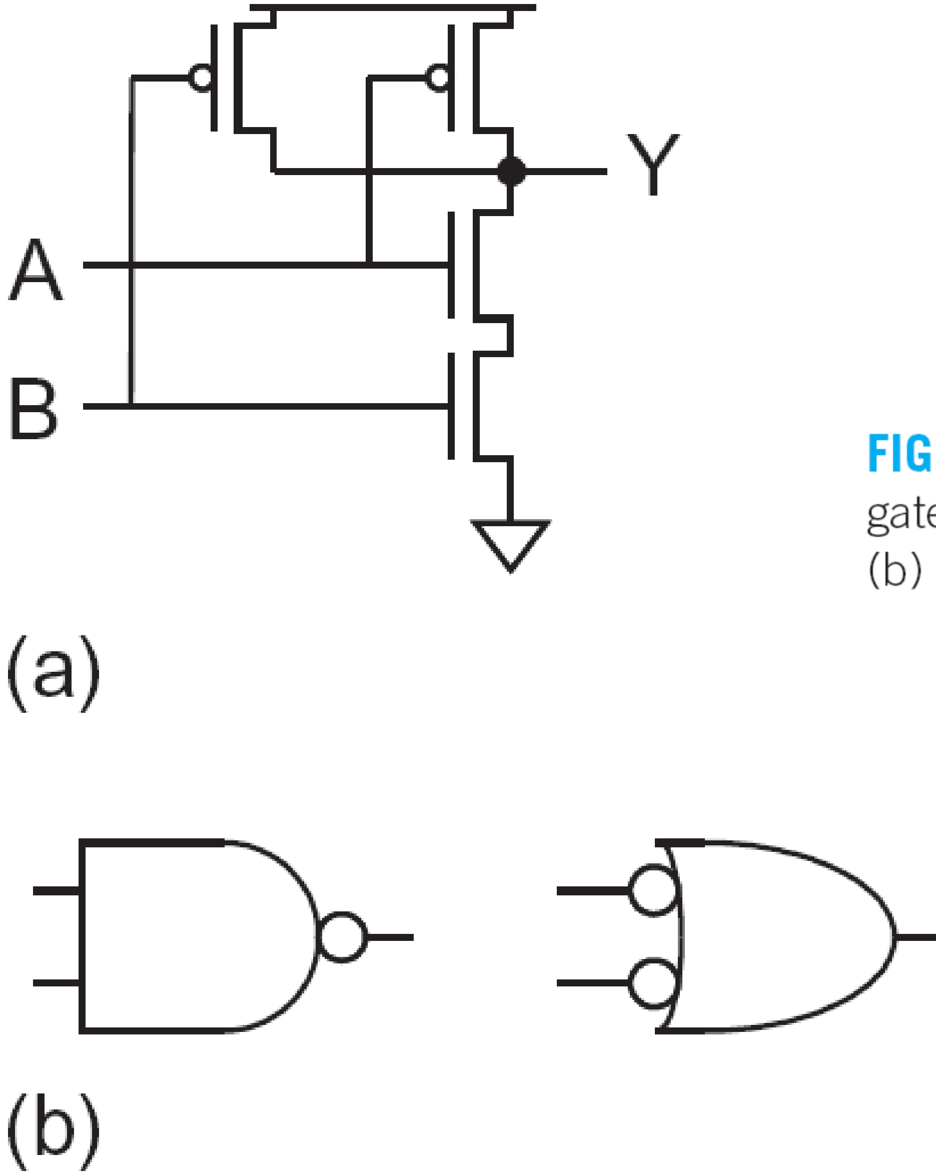


FIGURE 1.12 2-input NAND gate schematic (a) and symbol (b) $Y = \overline{A \cdot B}$

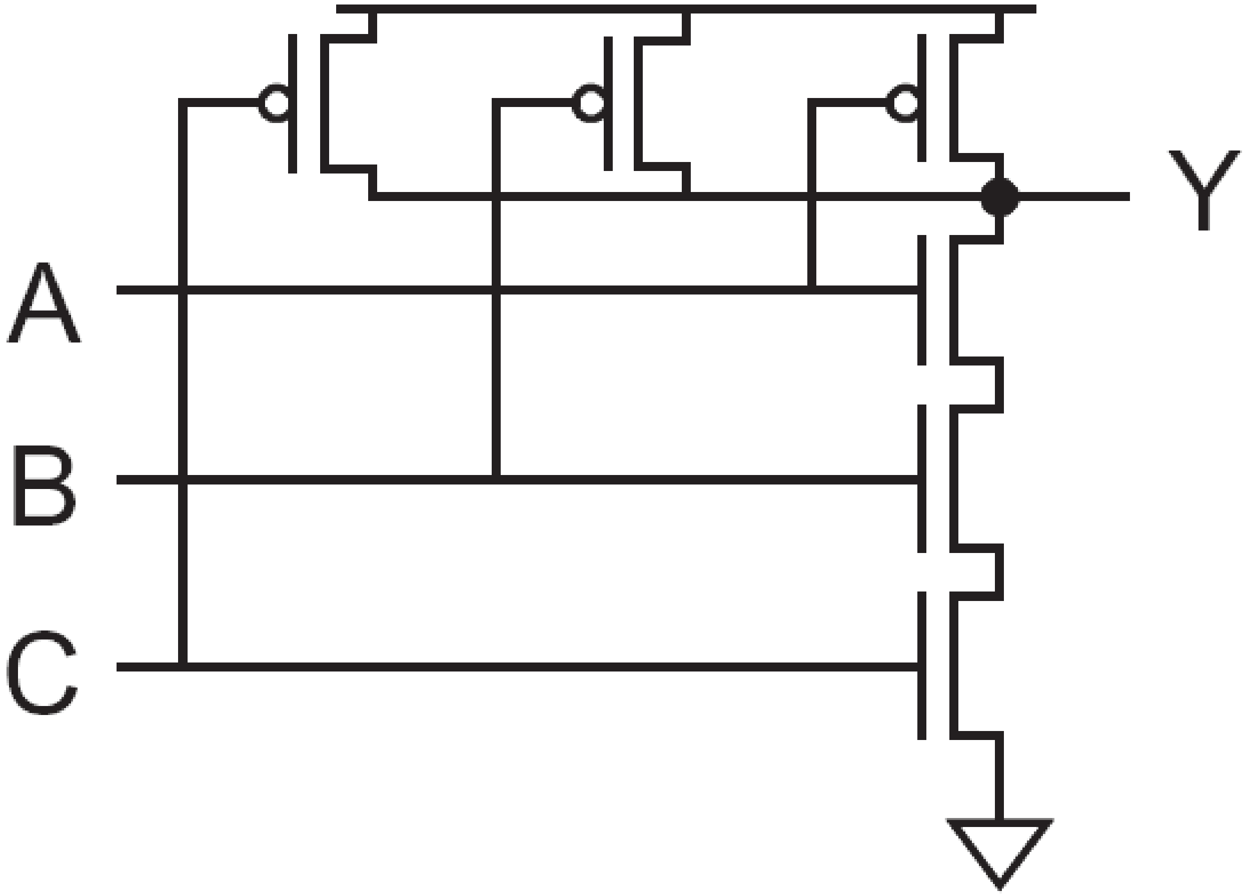


FIGURE 1.13 3-input NAND gate schematic $Y = \overline{A \cdot B \cdot C}$

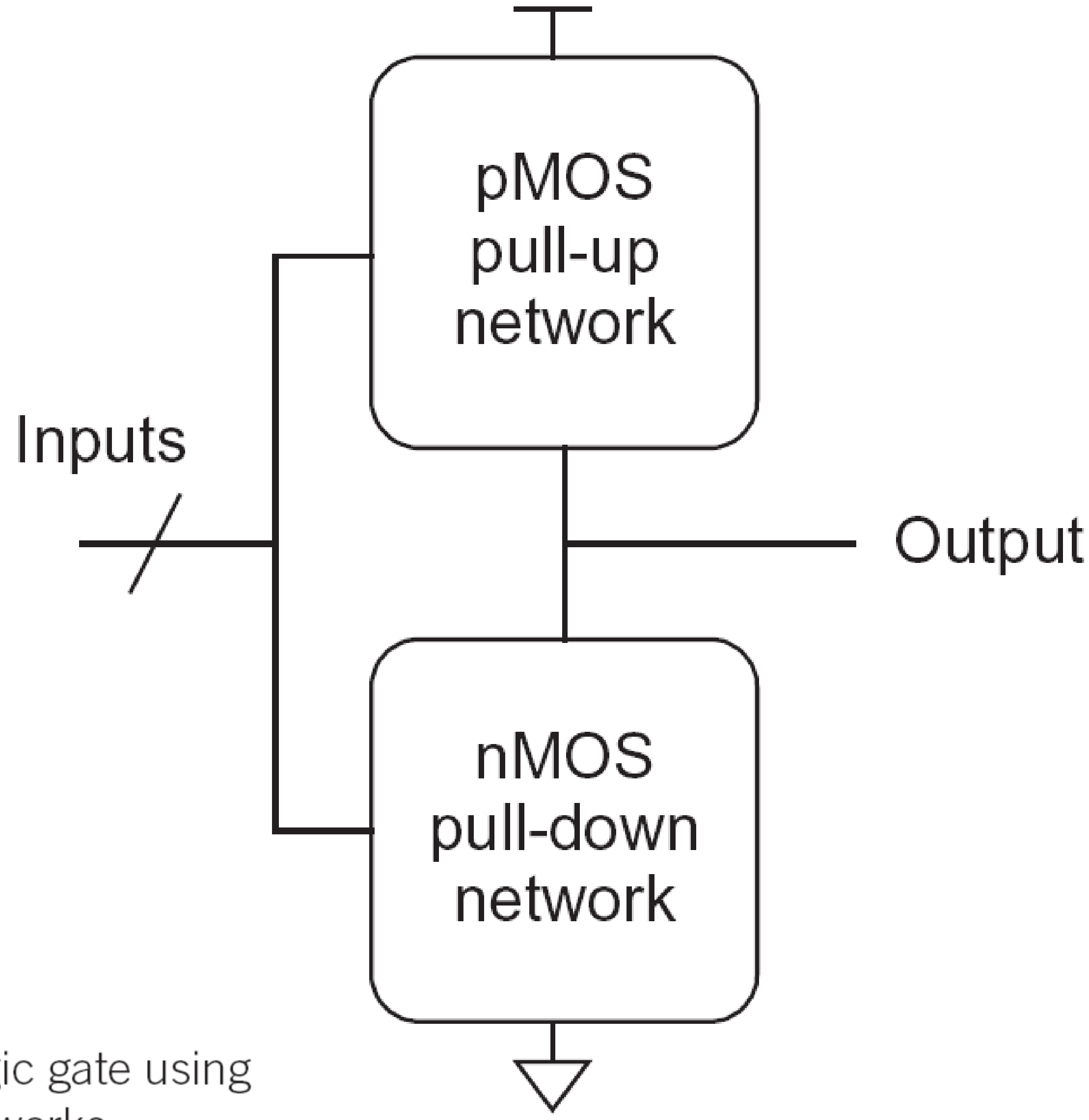


FIGURE 1.14 General logic gate using pull-up and pull-down networks

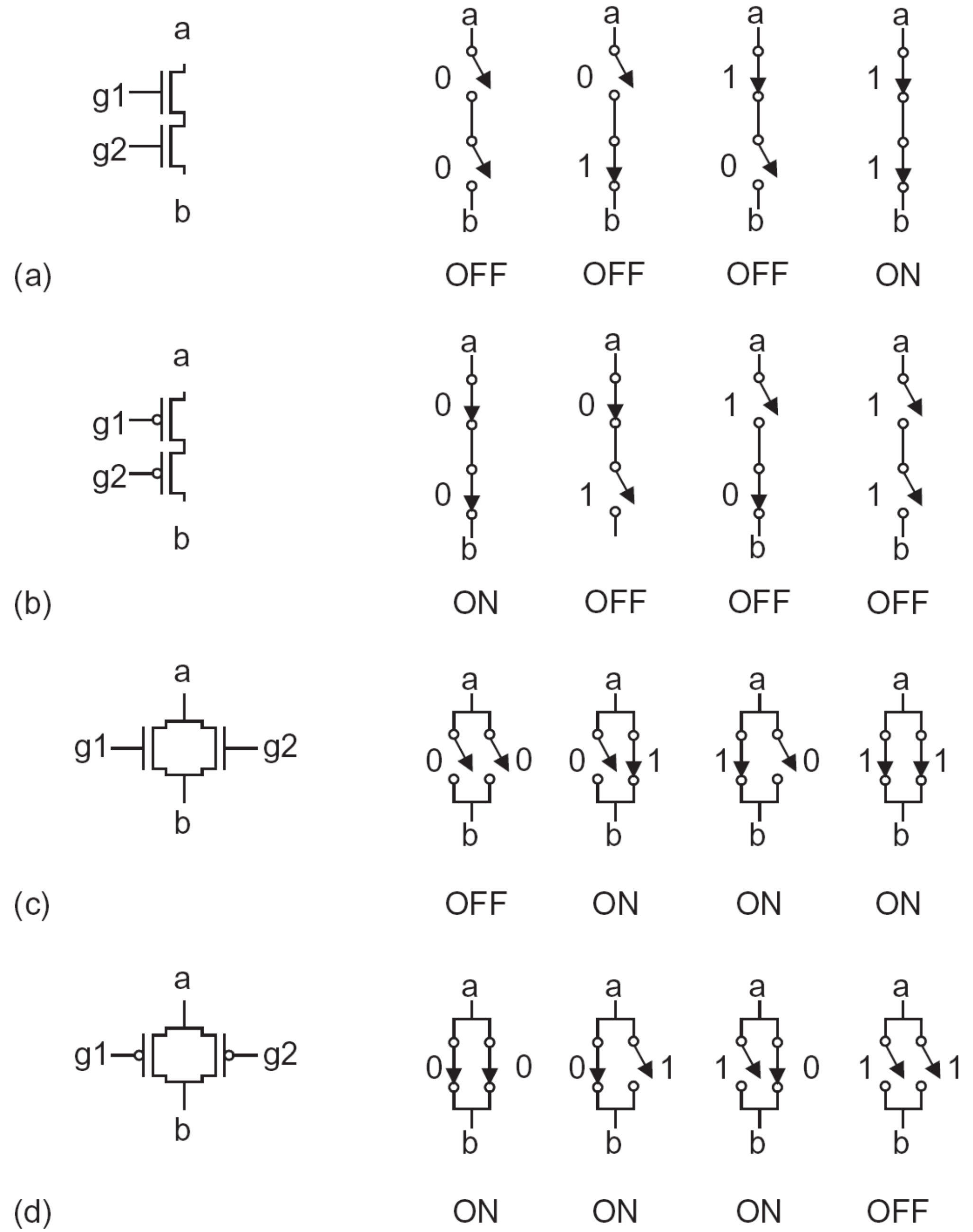
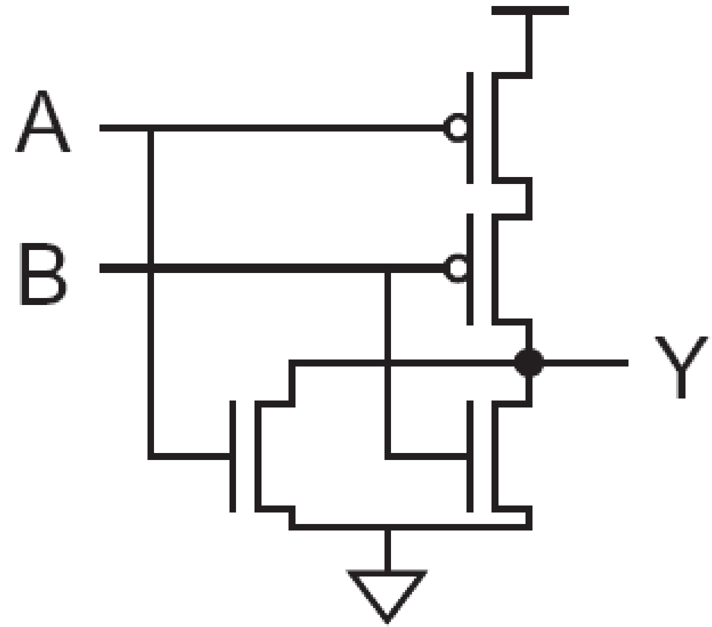
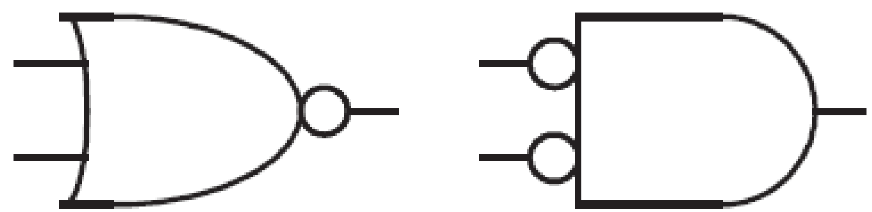


FIGURE 1.15

Connection and behavior of series and parallel transistors



(a)



(b)

FIGURE 1.16 2-input NOR gate schematic (a) and symbol (b) $Y = \overline{A + B}$

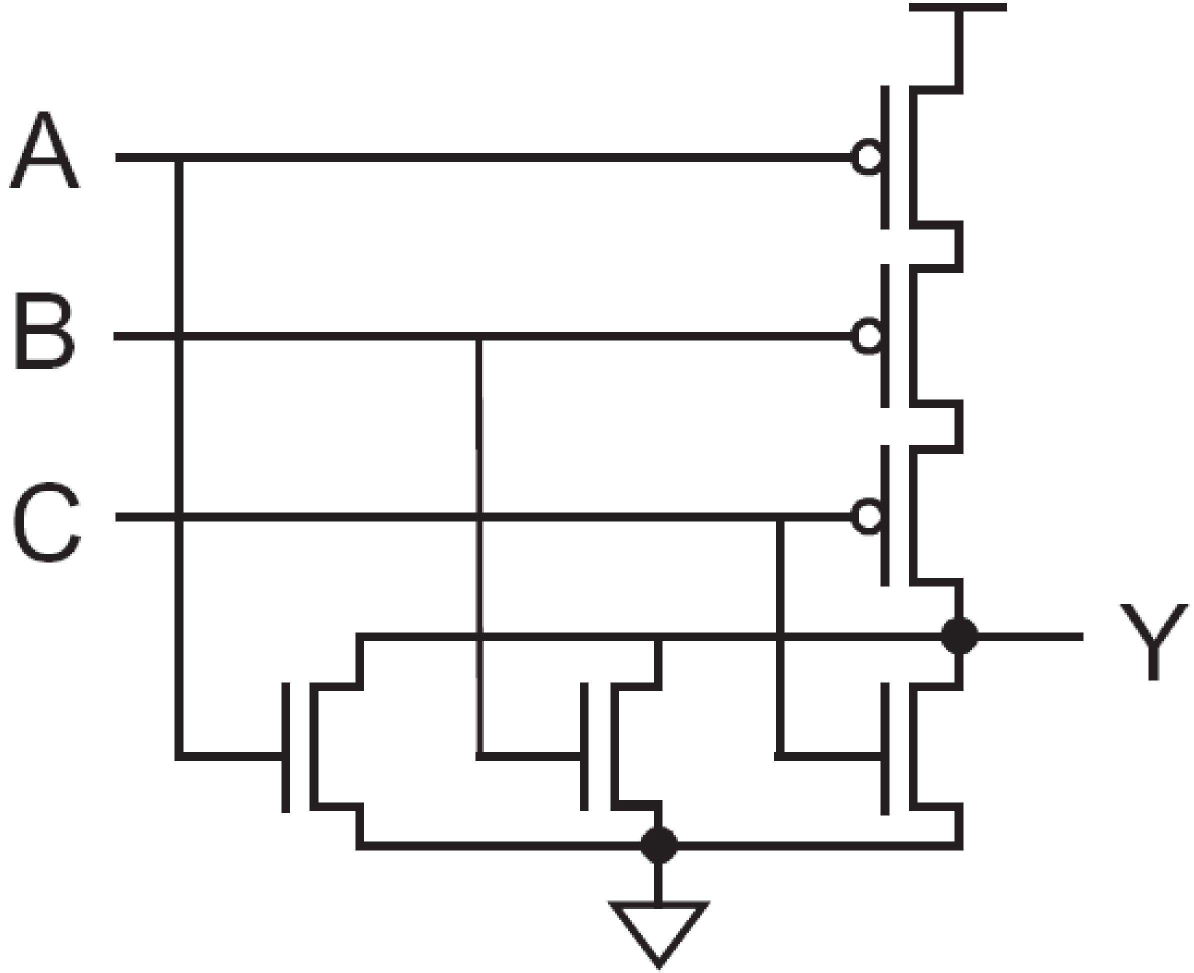


FIGURE 1.17 3-input NOR gate schematic $Y = \overline{A + B + C}$

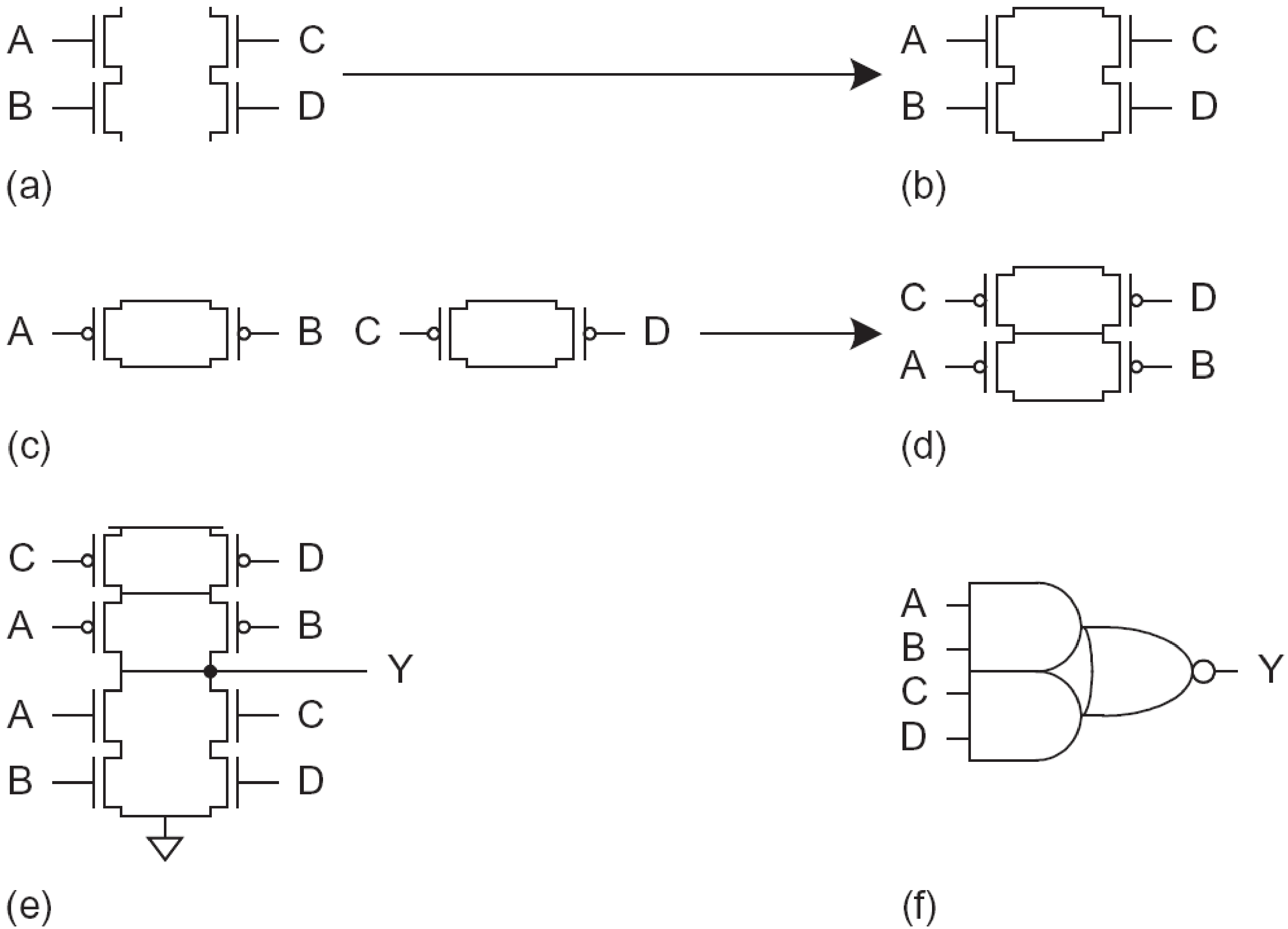


FIGURE 1.18 CMOS compound gate for function $Y = \overline{(A \cdot B) + (C \cdot D)}$

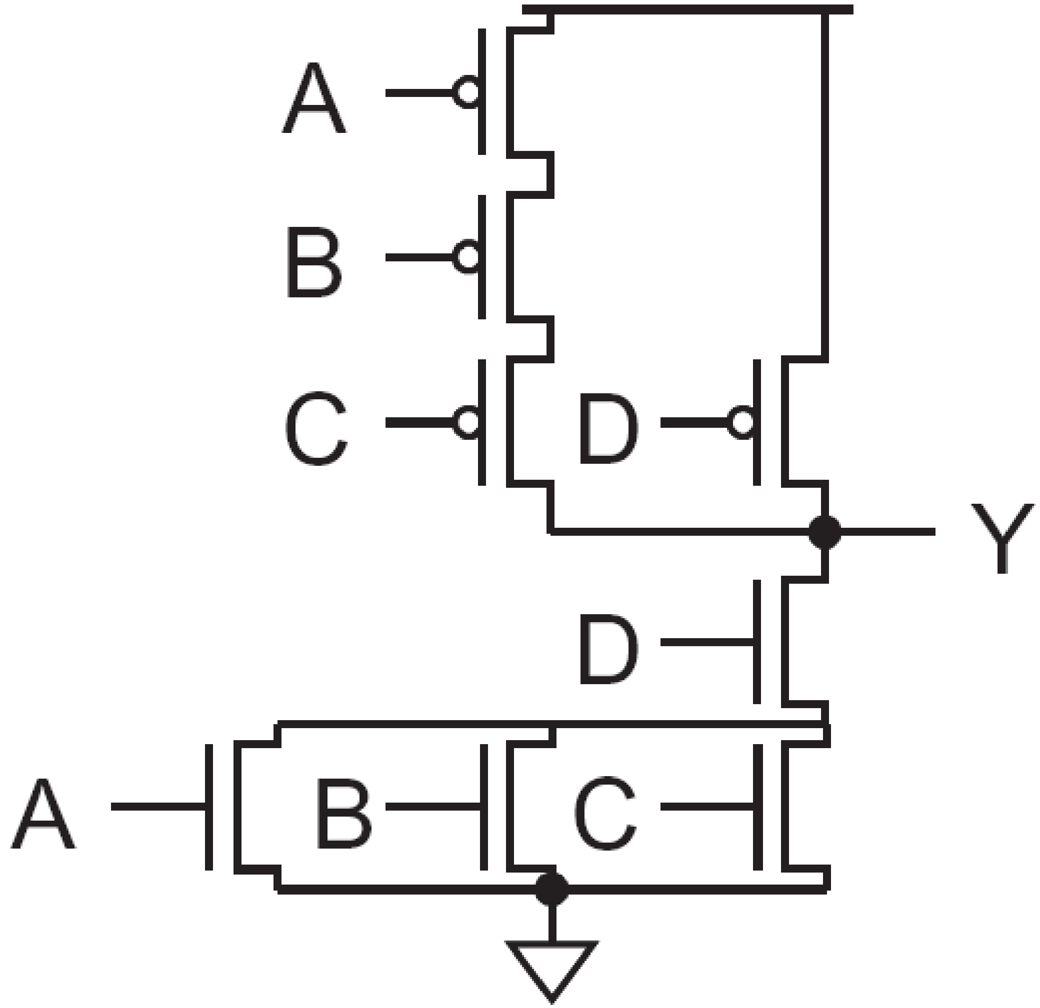


FIGURE 1.19
CMOS compound gate for function
$Y = \overline{(A + B + C) \cdot D}$

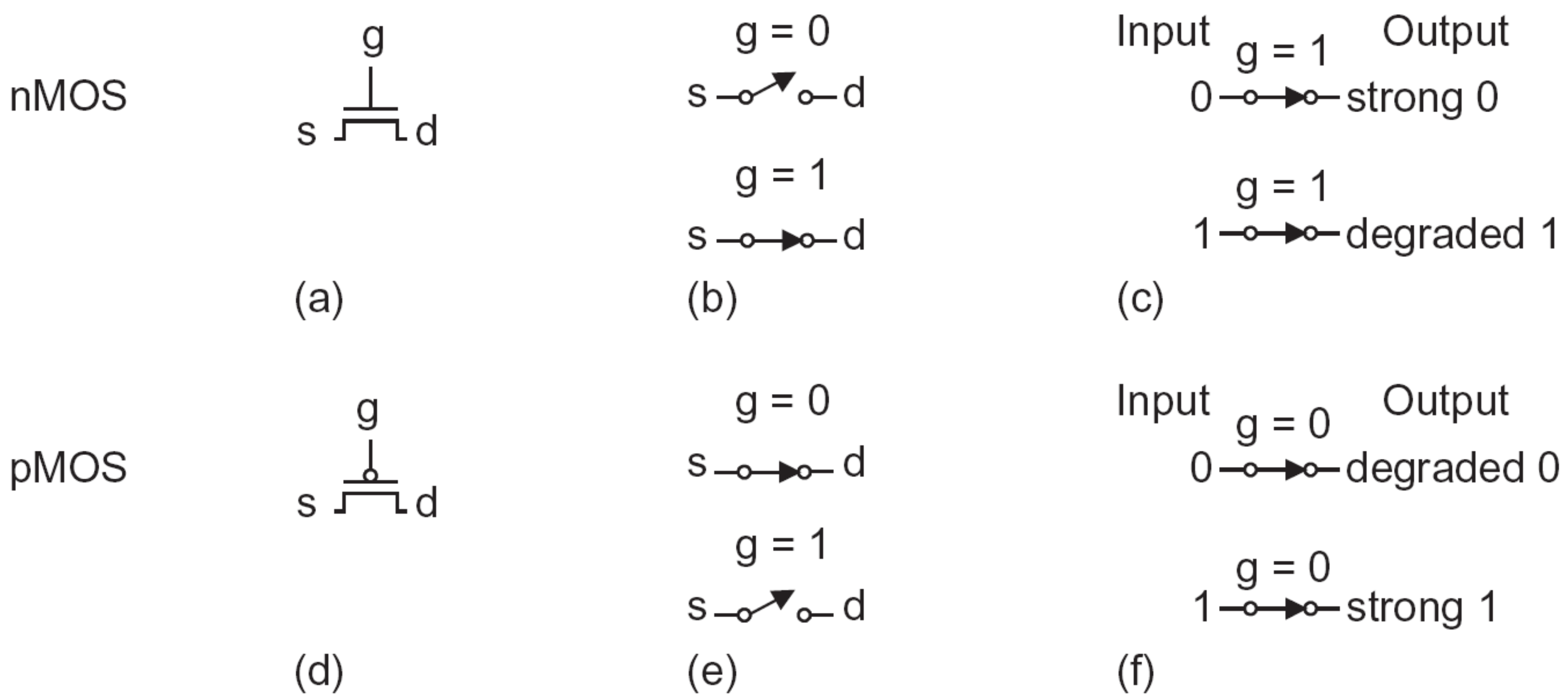


FIGURE 1.20 Pass transistor strong and degraded outputs

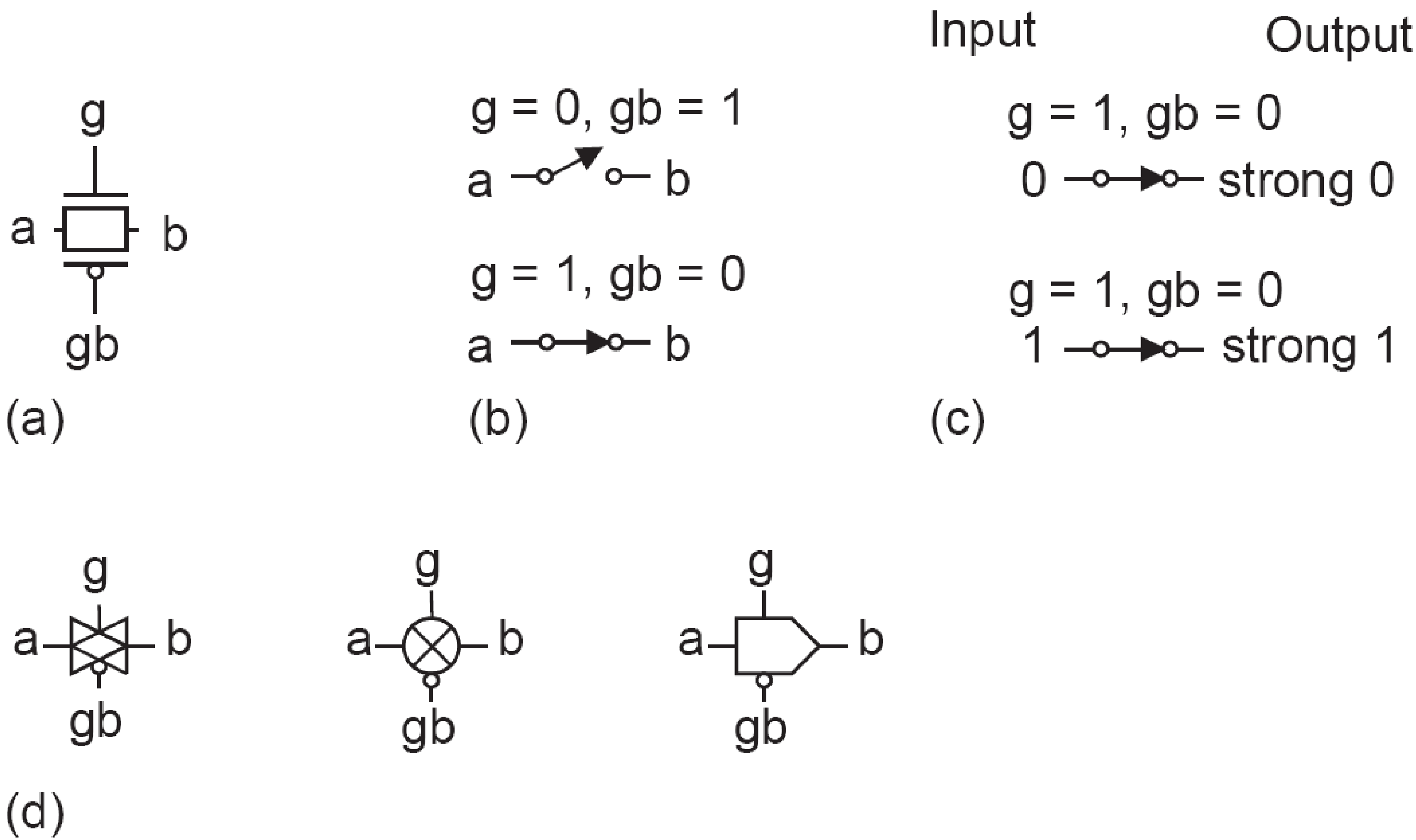


FIGURE 1.21 Transmission gate

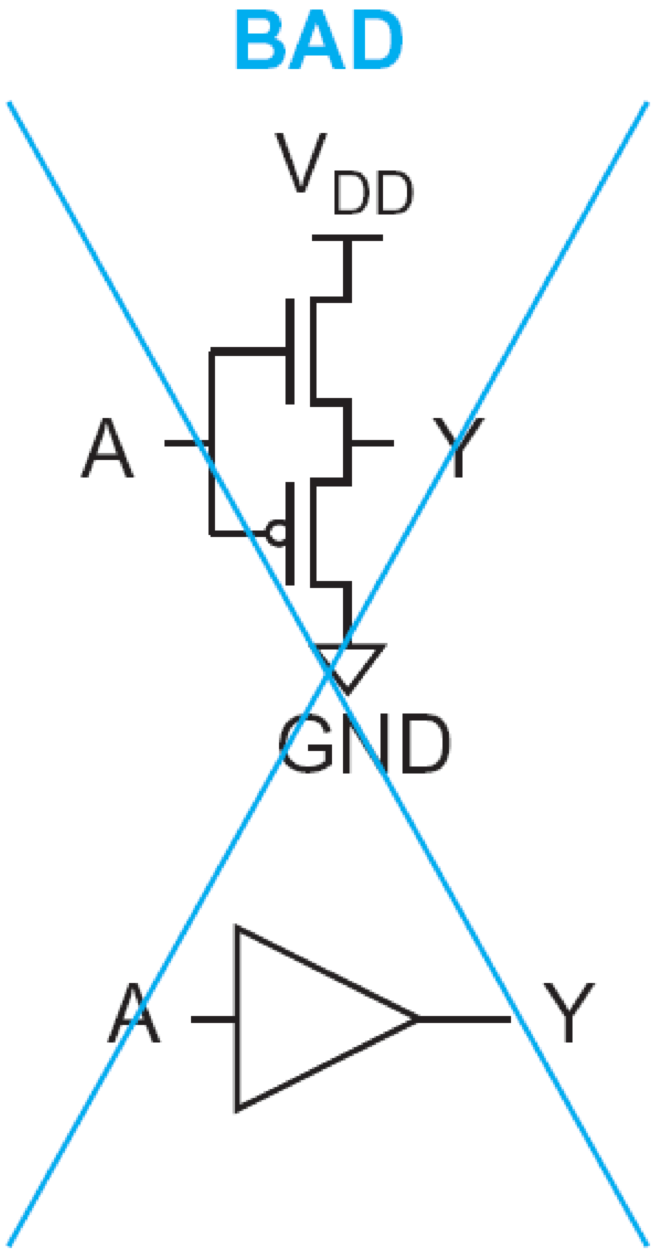


FIGURE 1.22
Bad noninverting buffer

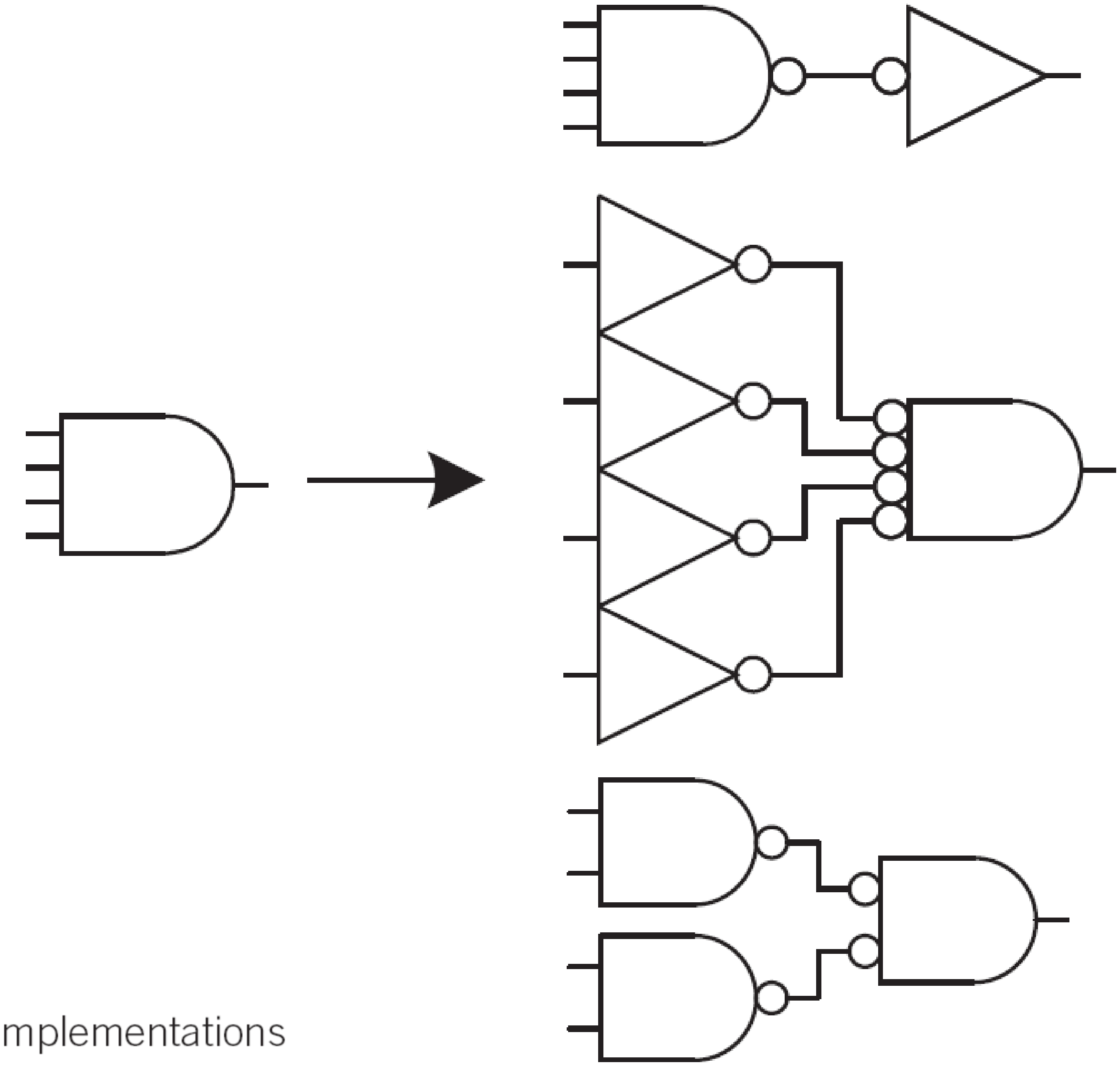


FIGURE 1.23 Various implementations of a CMOS 4-input AND gate

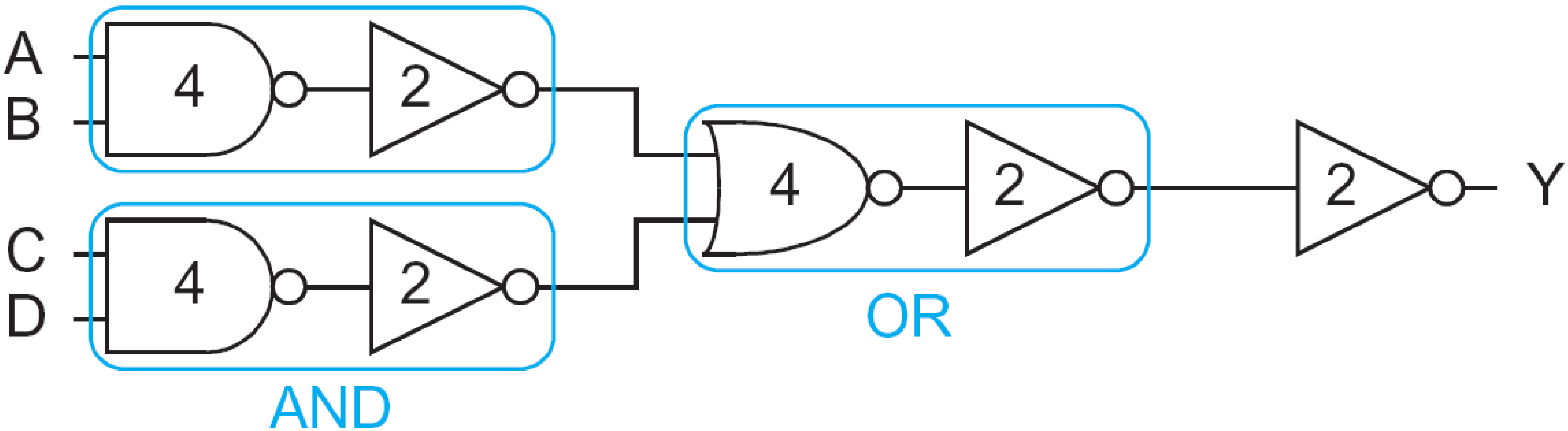


FIGURE 1.24 Inefficient discrete gate implementation of AOI22 with transistor counts indicated

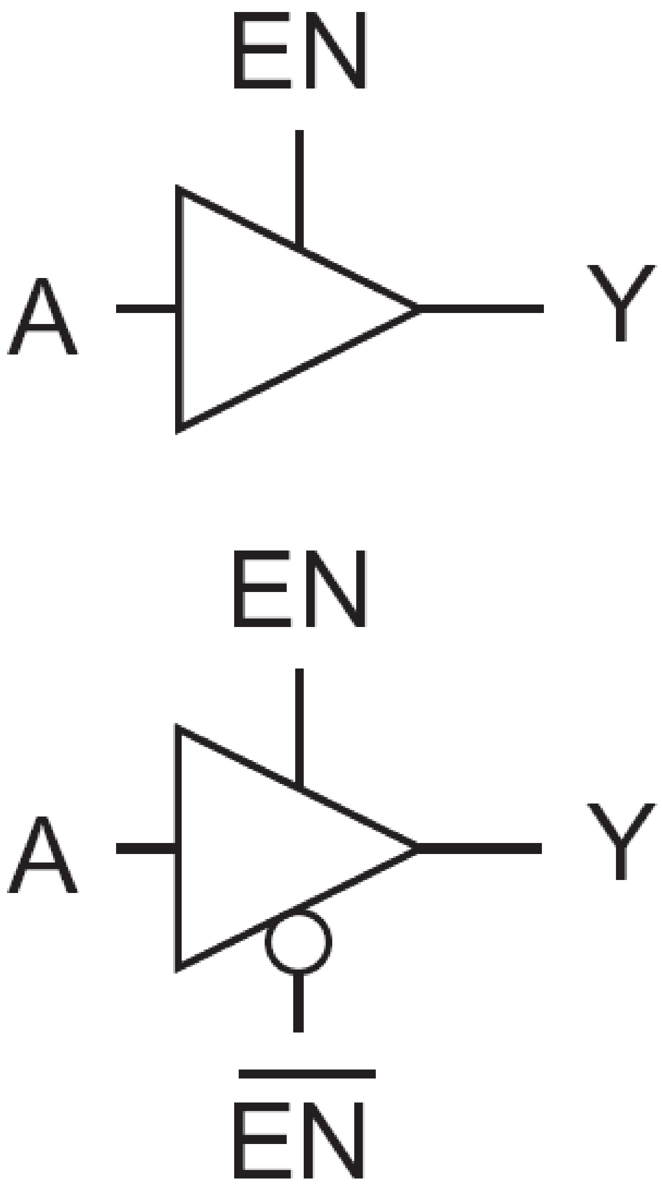


FIGURE 1.25
Tristate buffer symbol

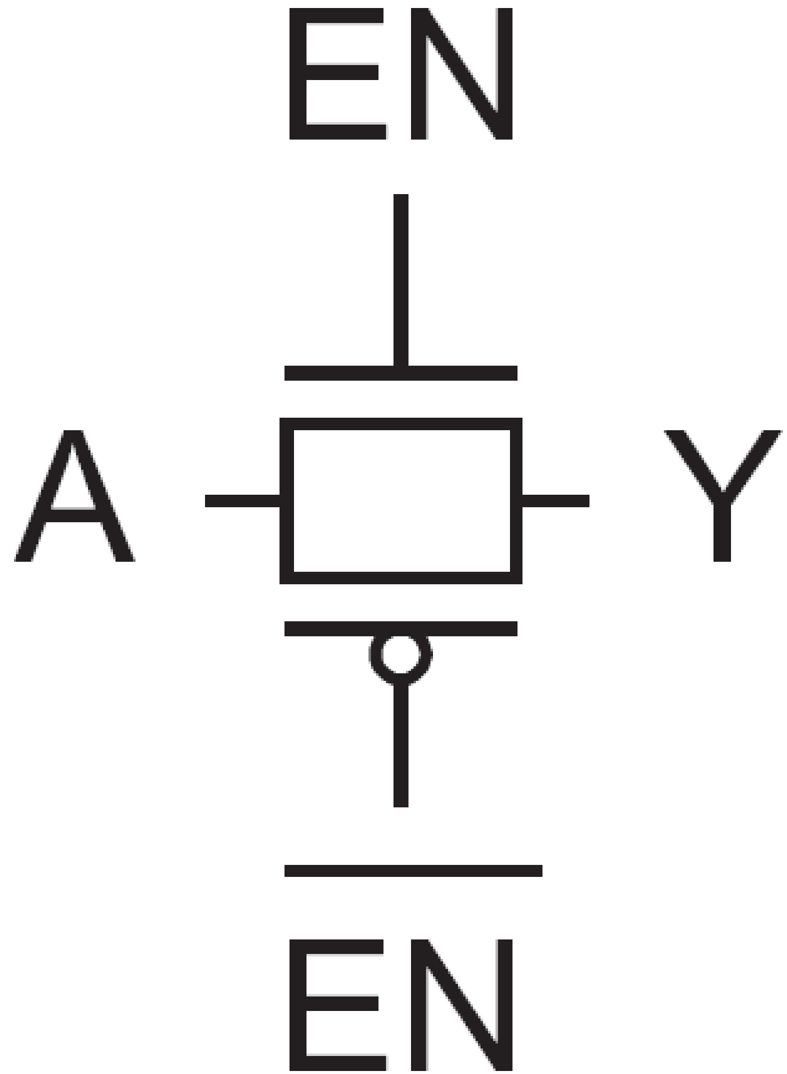


FIGURE 1.26
Transmission gate

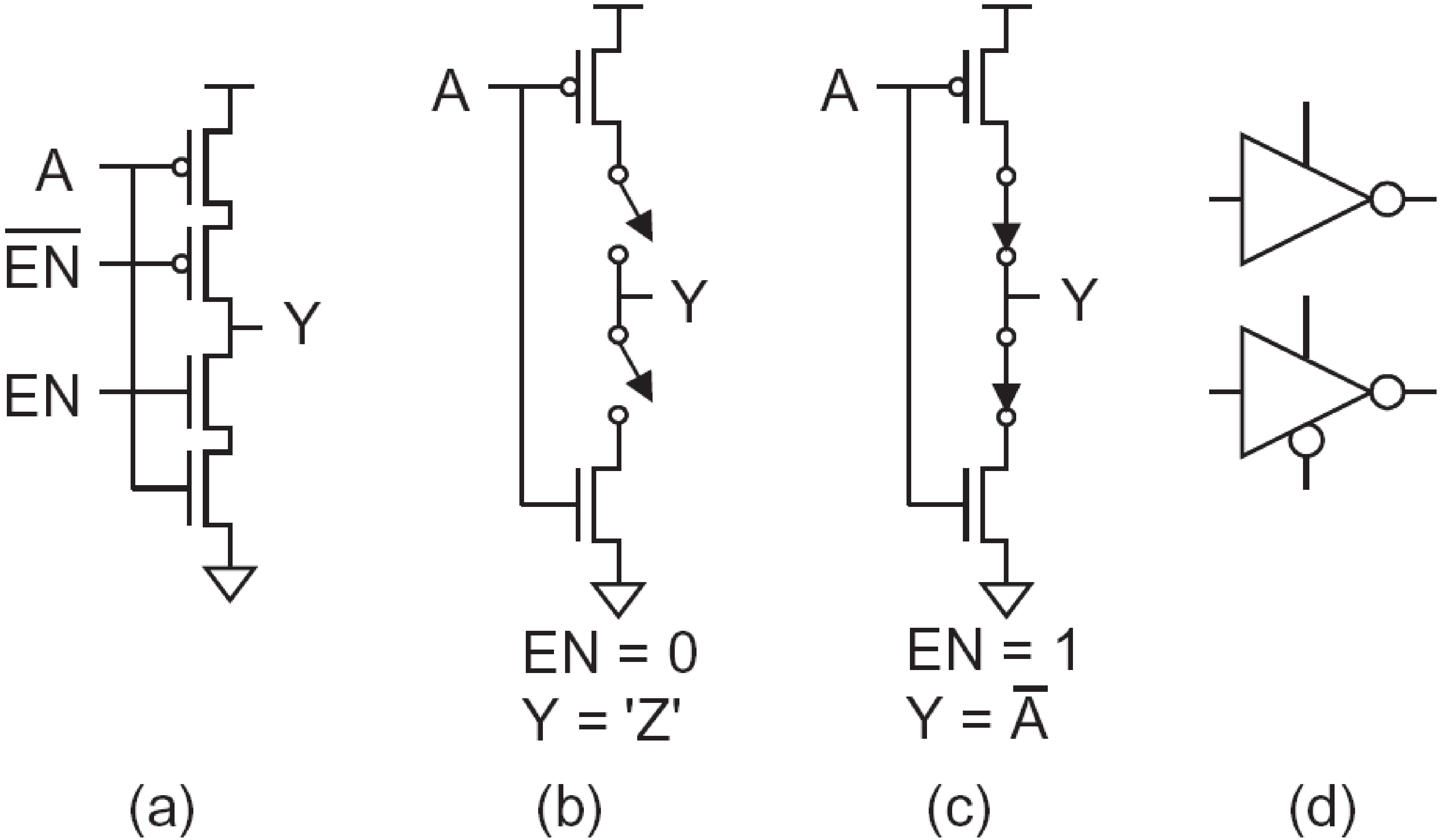


FIGURE 1.27 Tristate Inverter

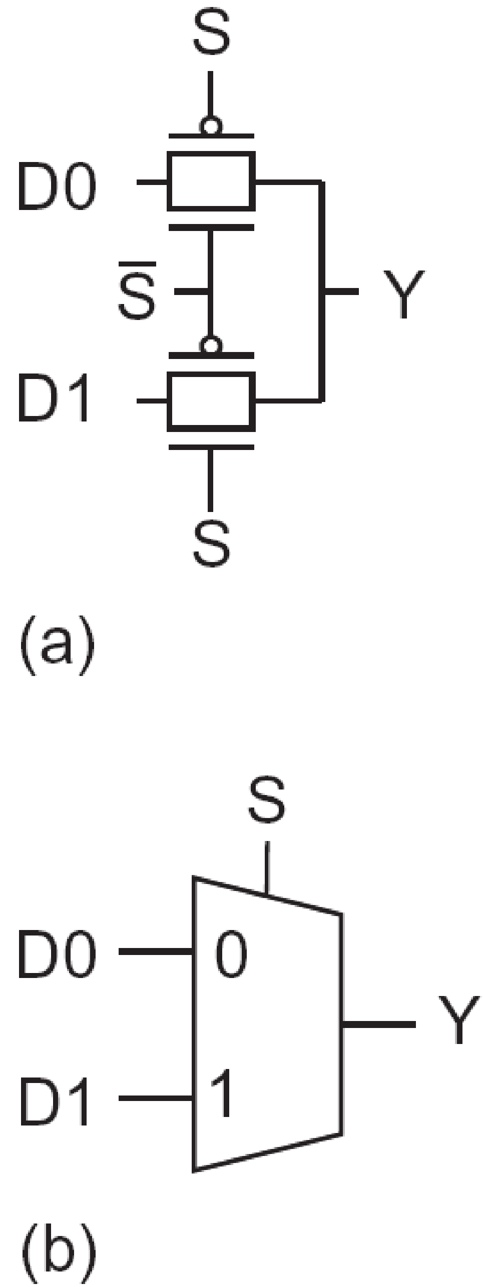


FIGURE 1.28 Transmission gate multiplexer

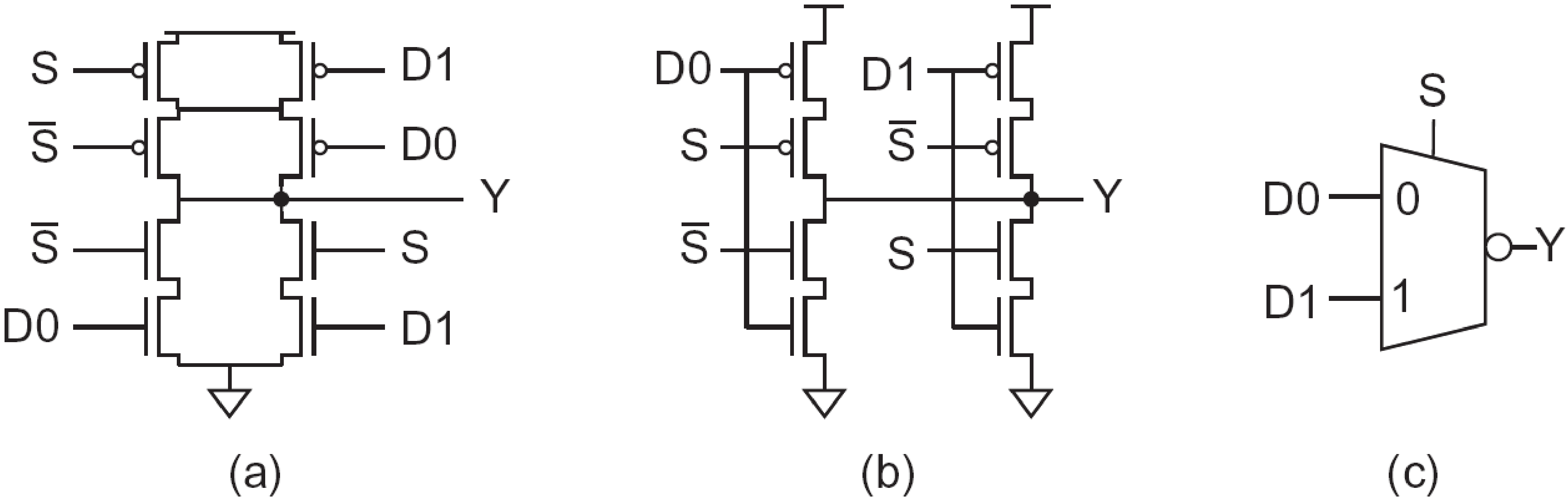
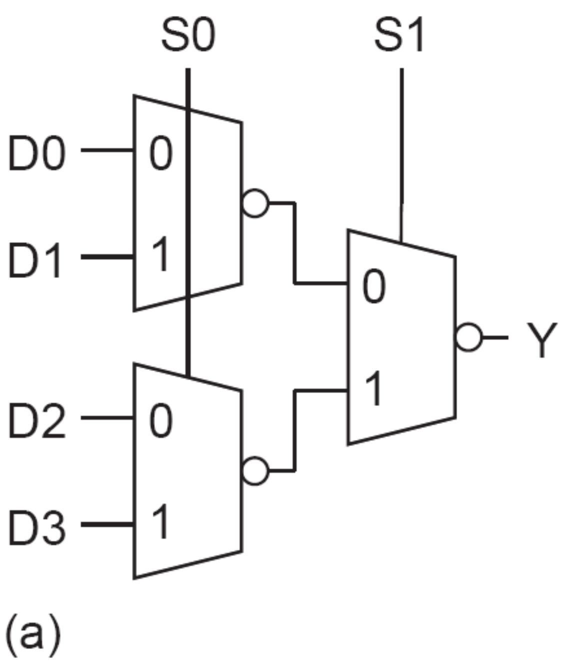
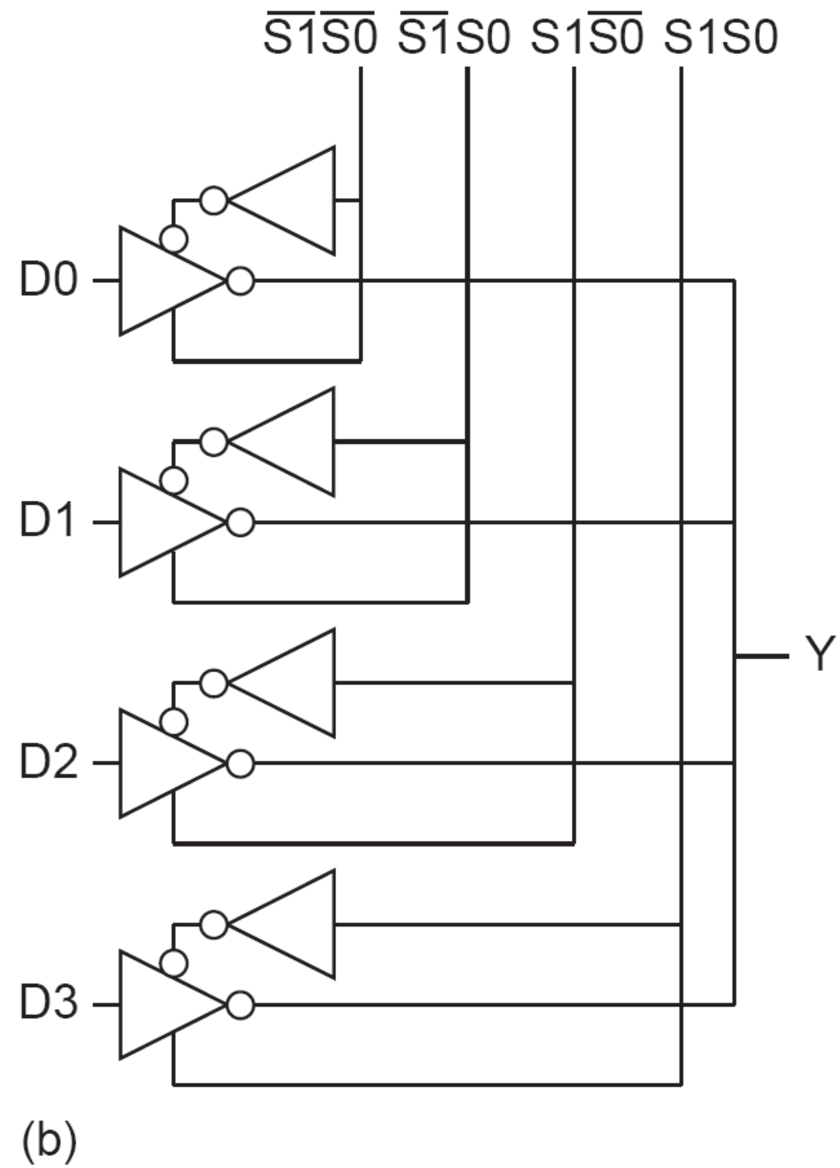


FIGURE 1.29 Inverting multiplexer

FIGURE 1.30 4:1 multiplexer





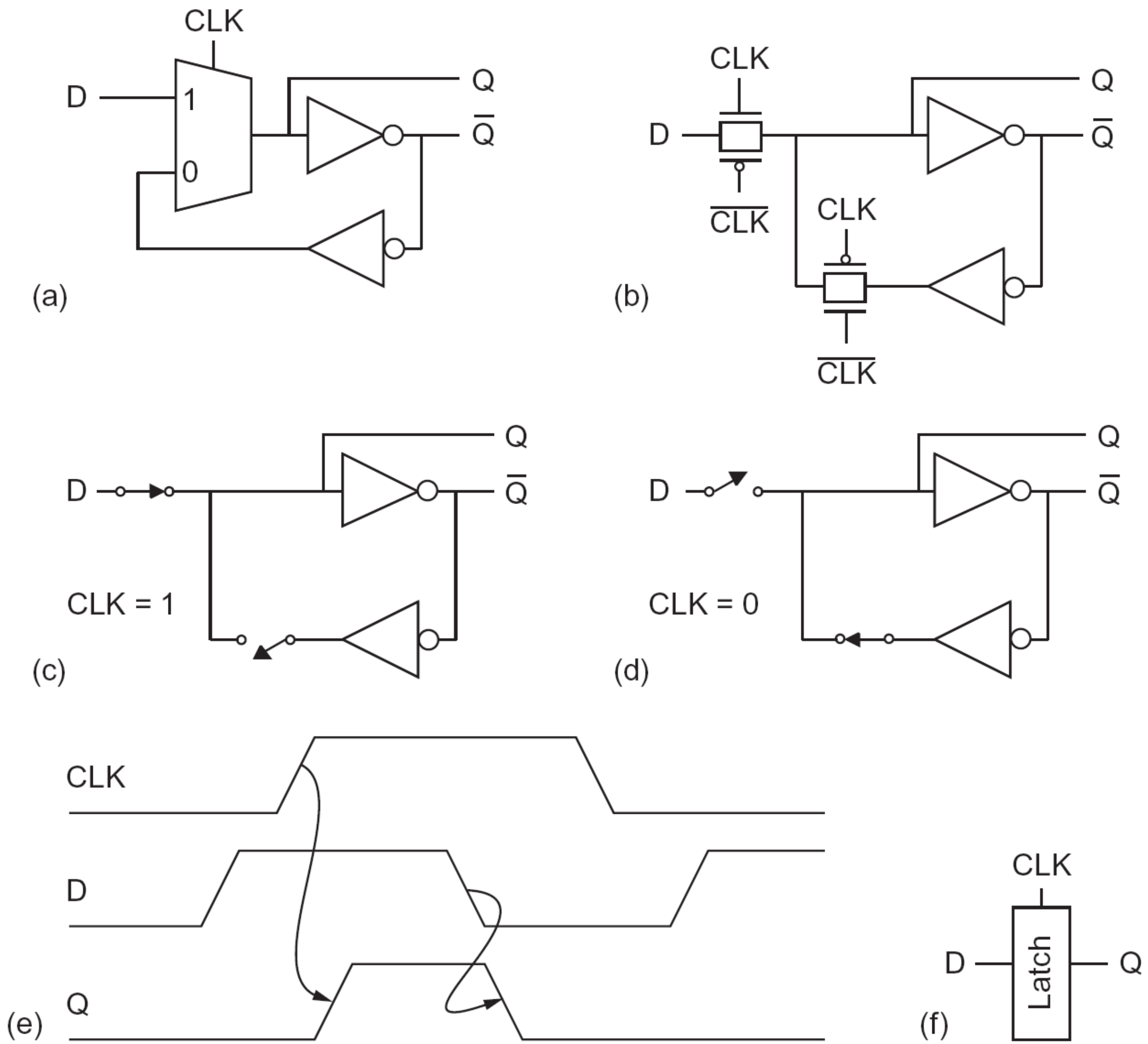


FIGURE 1.31 CMOS positive-level-sensitive *D* latch

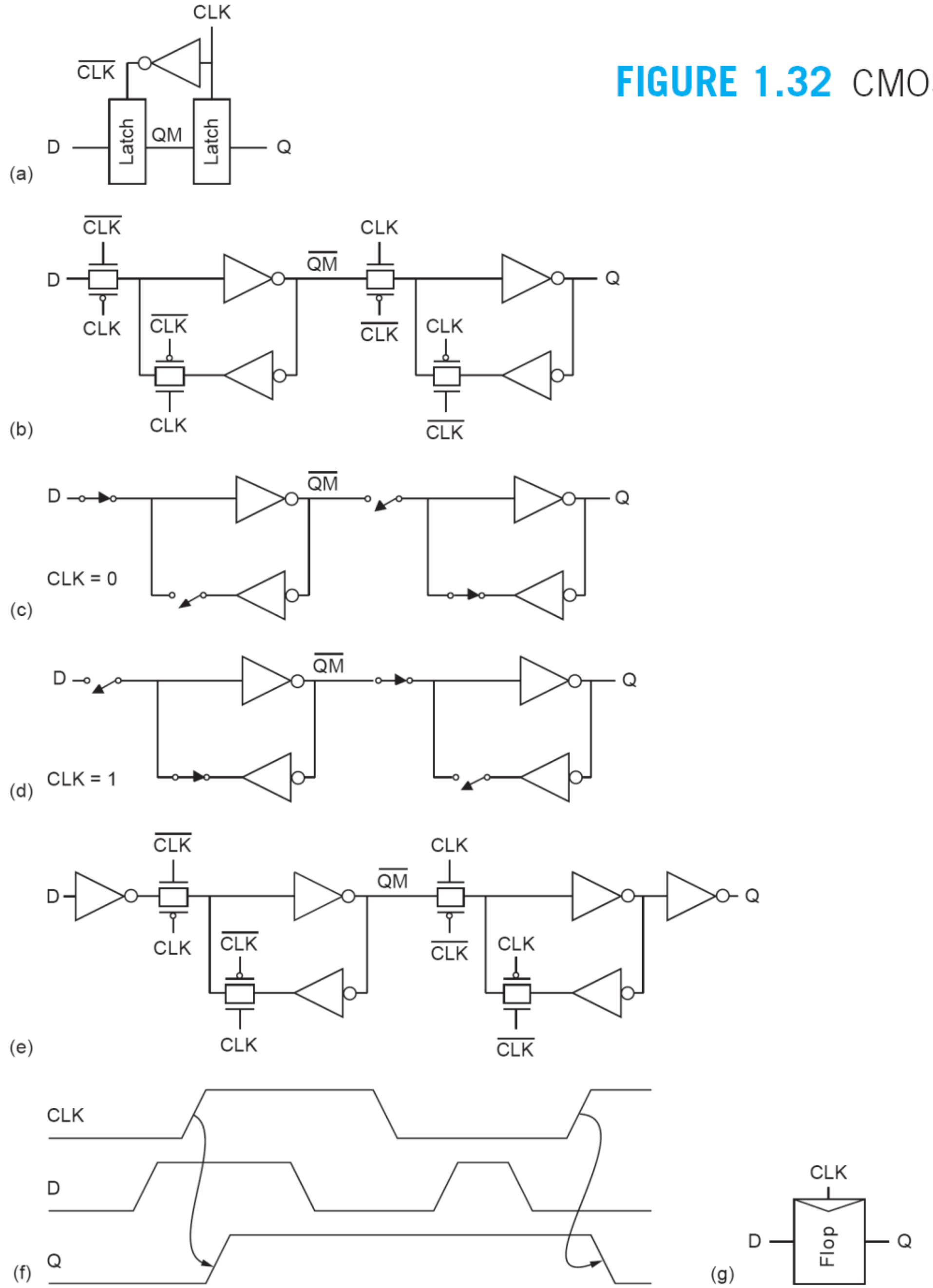


FIGURE 1.32 CMOS positive-edge-triggered *D* flip-flop

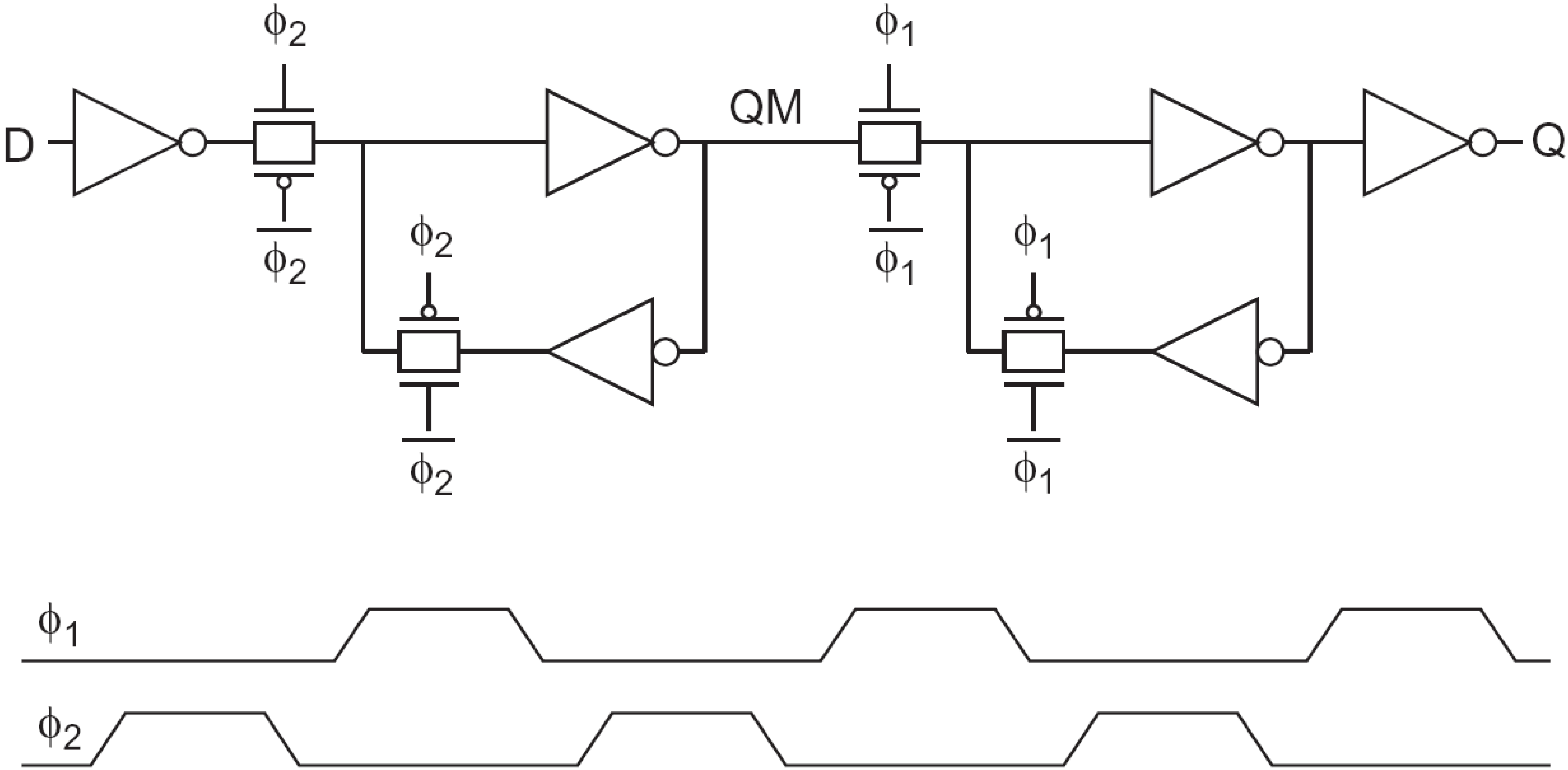


FIGURE 1.33 CMOS flip-flop with two-phase nonoverlapping clocks

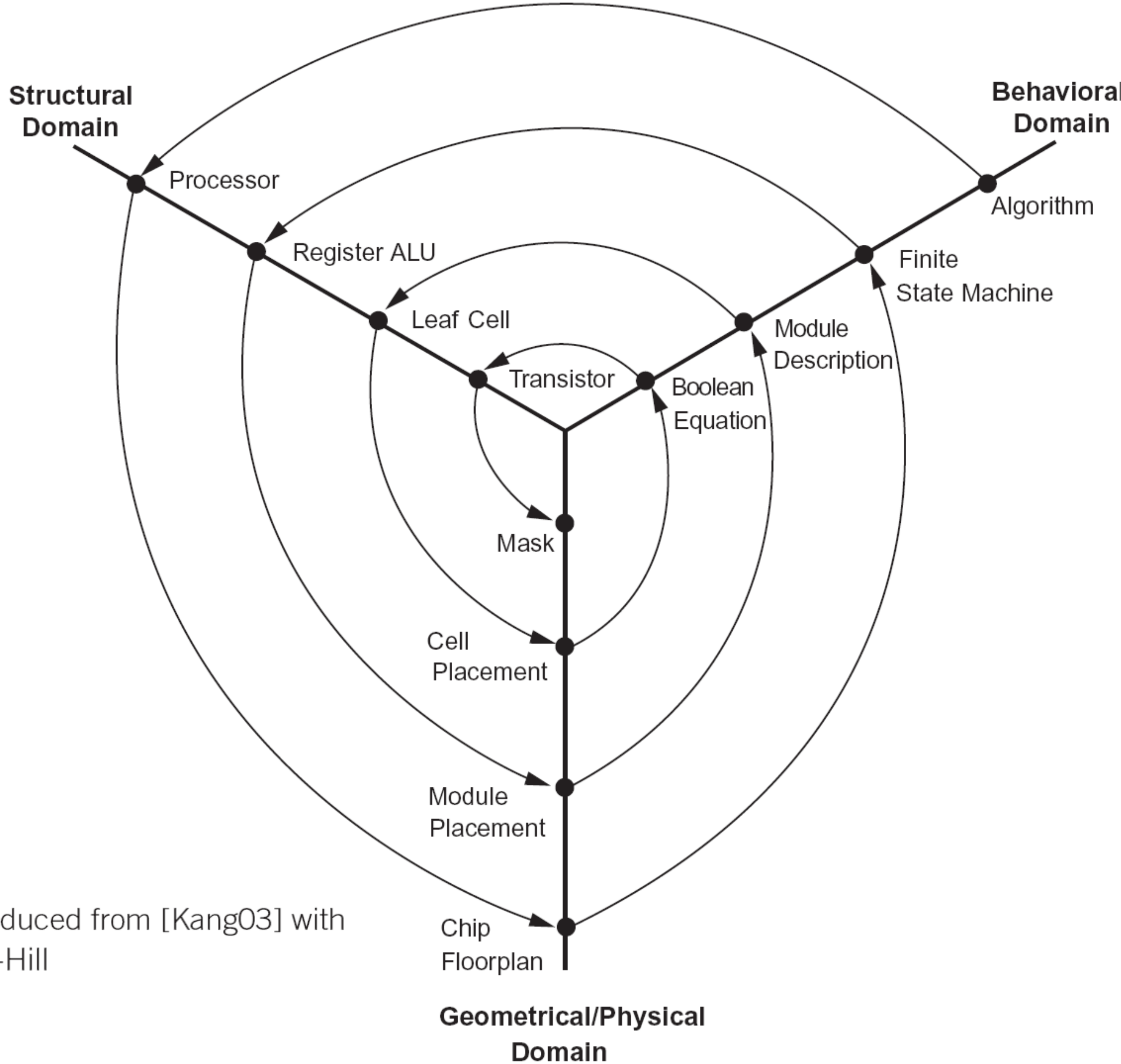


FIGURE 1.48 Y Diagram. Reproduced from [Kang03] with with permission of The McGraw-Hill Companies.

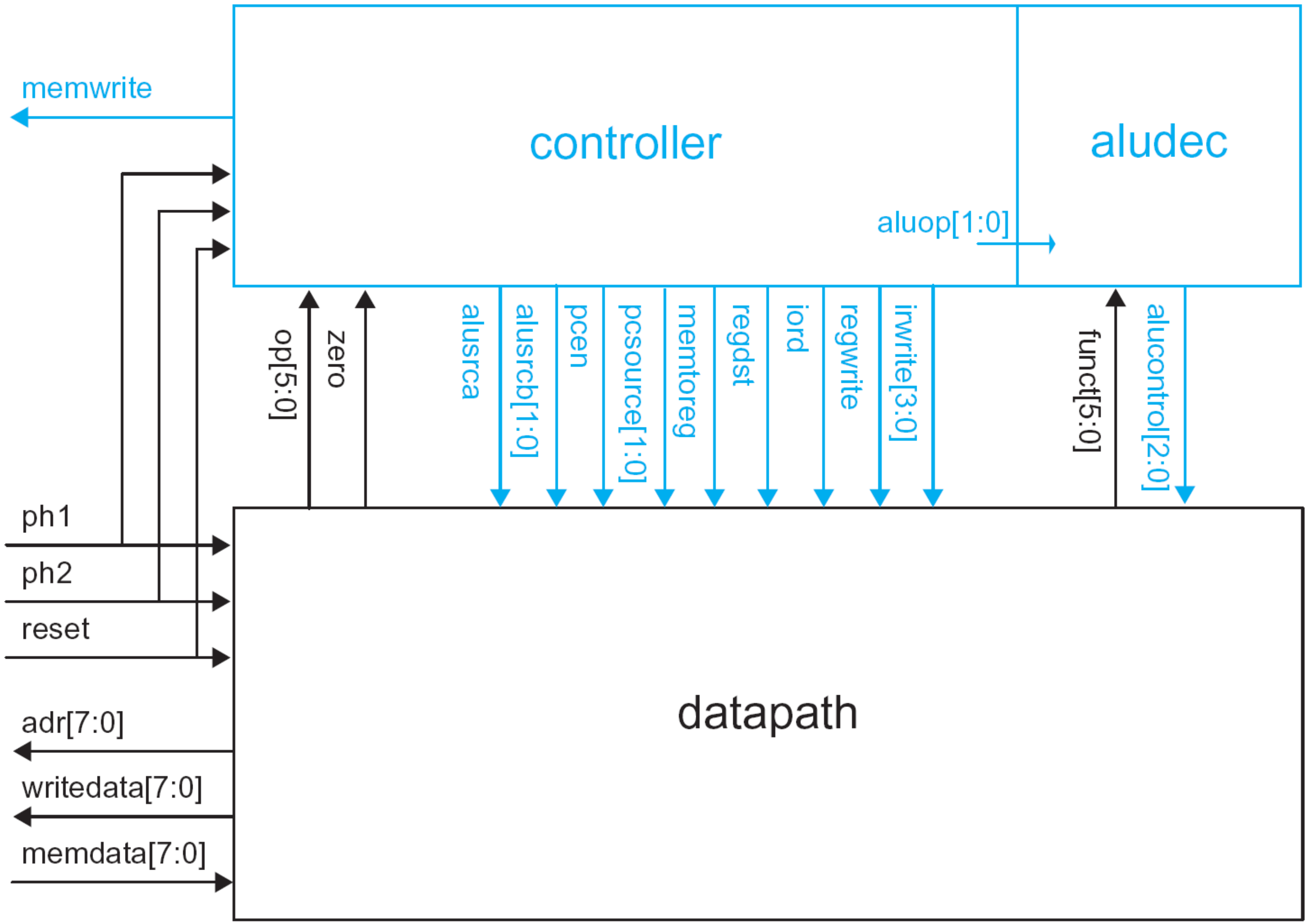


FIGURE 1.56 Top-level MIPS block diagram

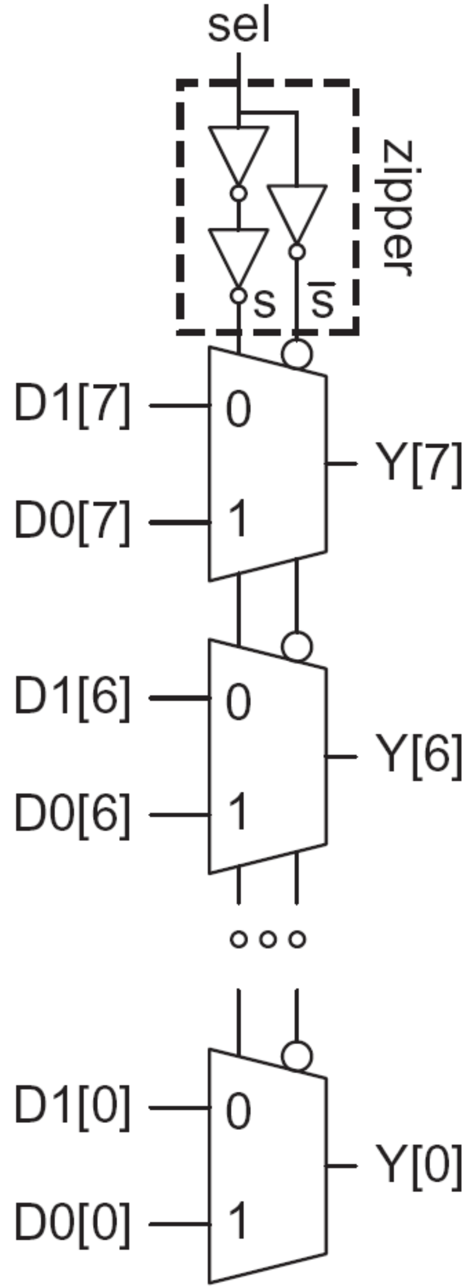


FIGURE 1.57 8-bit 2:1 multiplexer wordslice

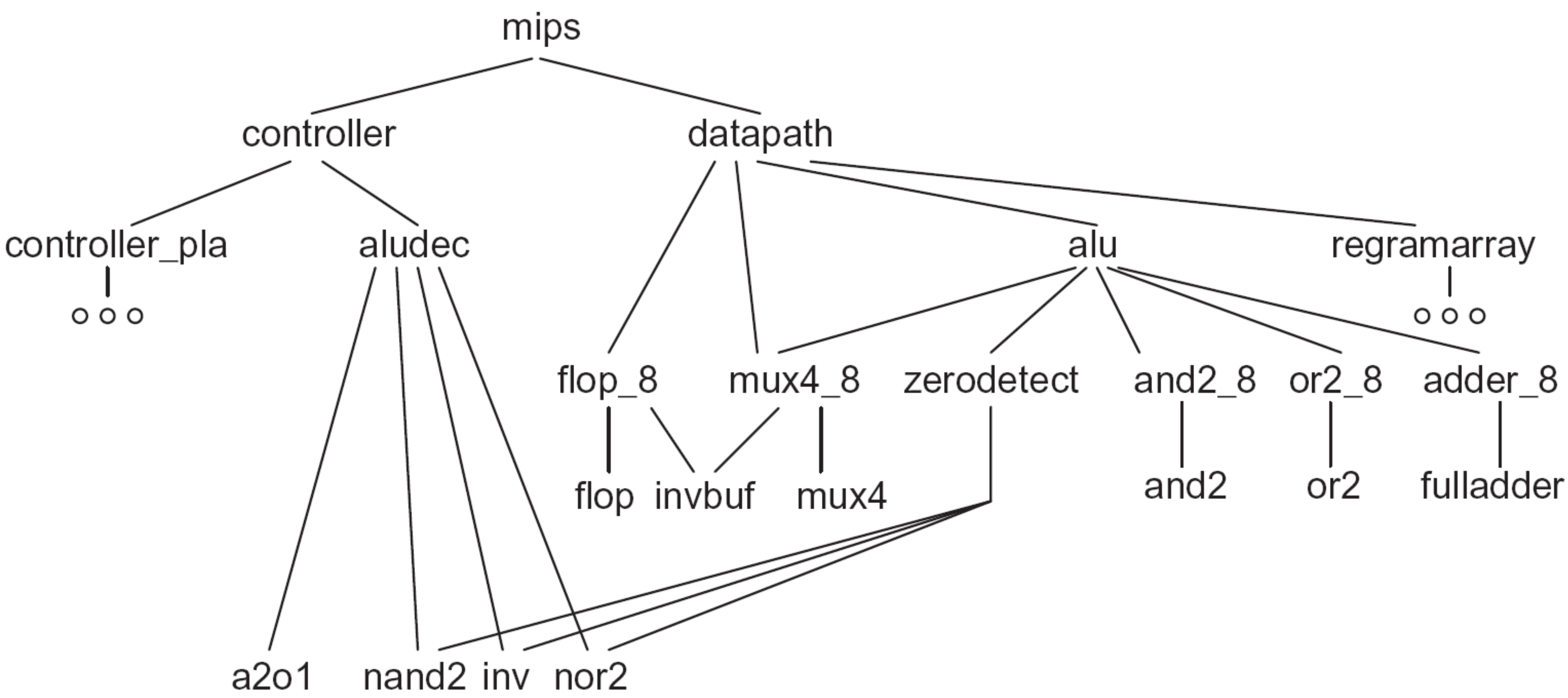


FIGURE 1.58 MIPS design hierarchy

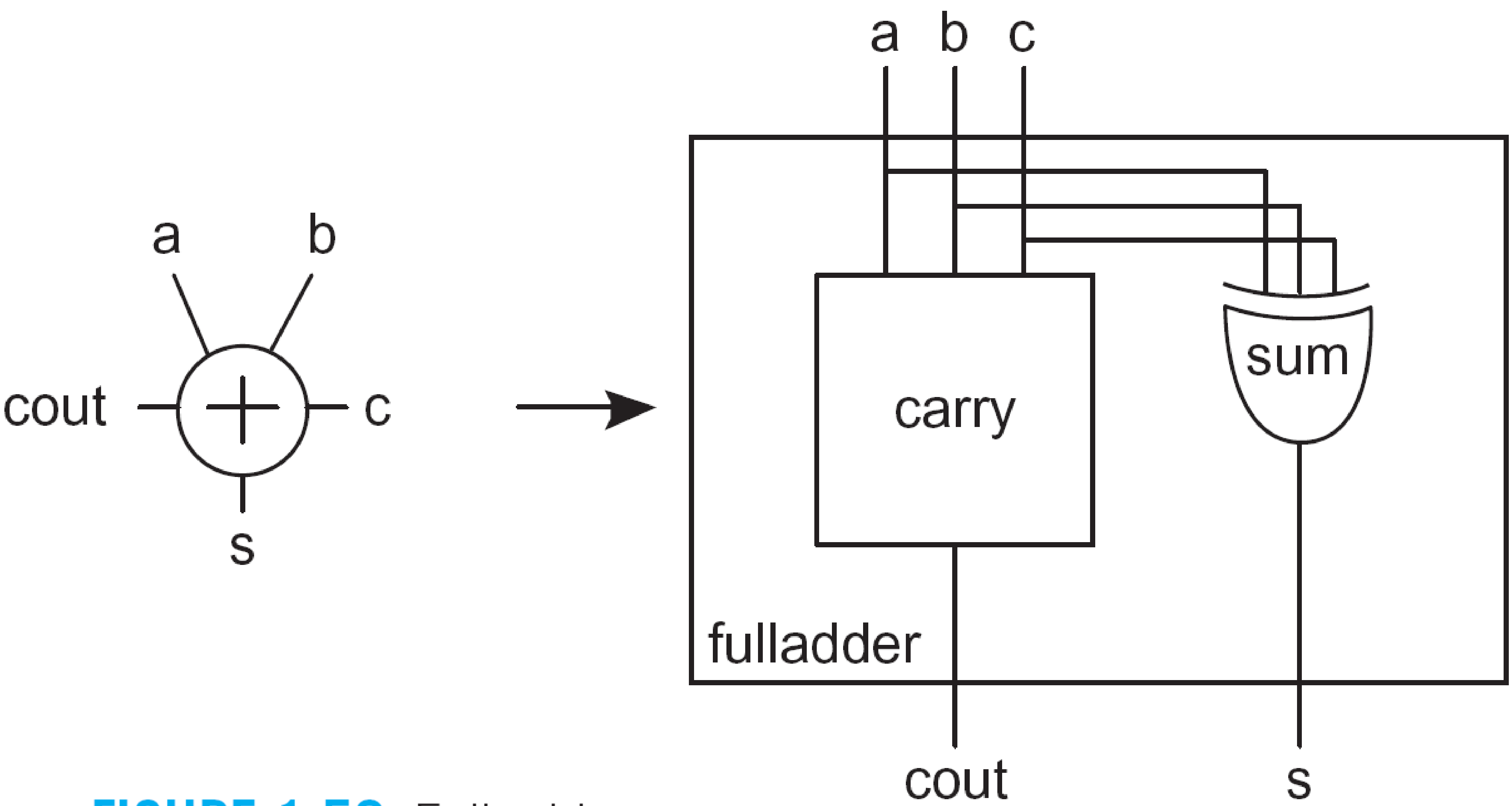


FIGURE 1.59 Full adder

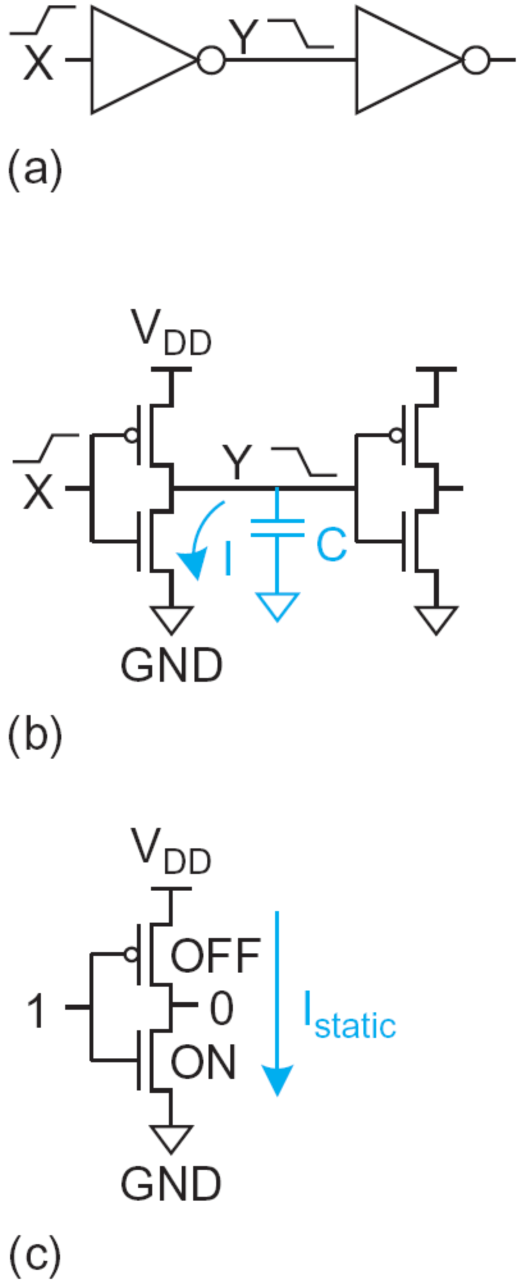


FIGURE 1.60 Circuit delay and power: (a) inverter pair, (b) transistor-level model showing capacitance and current during switching, (c) static leakage current during quiescent operation

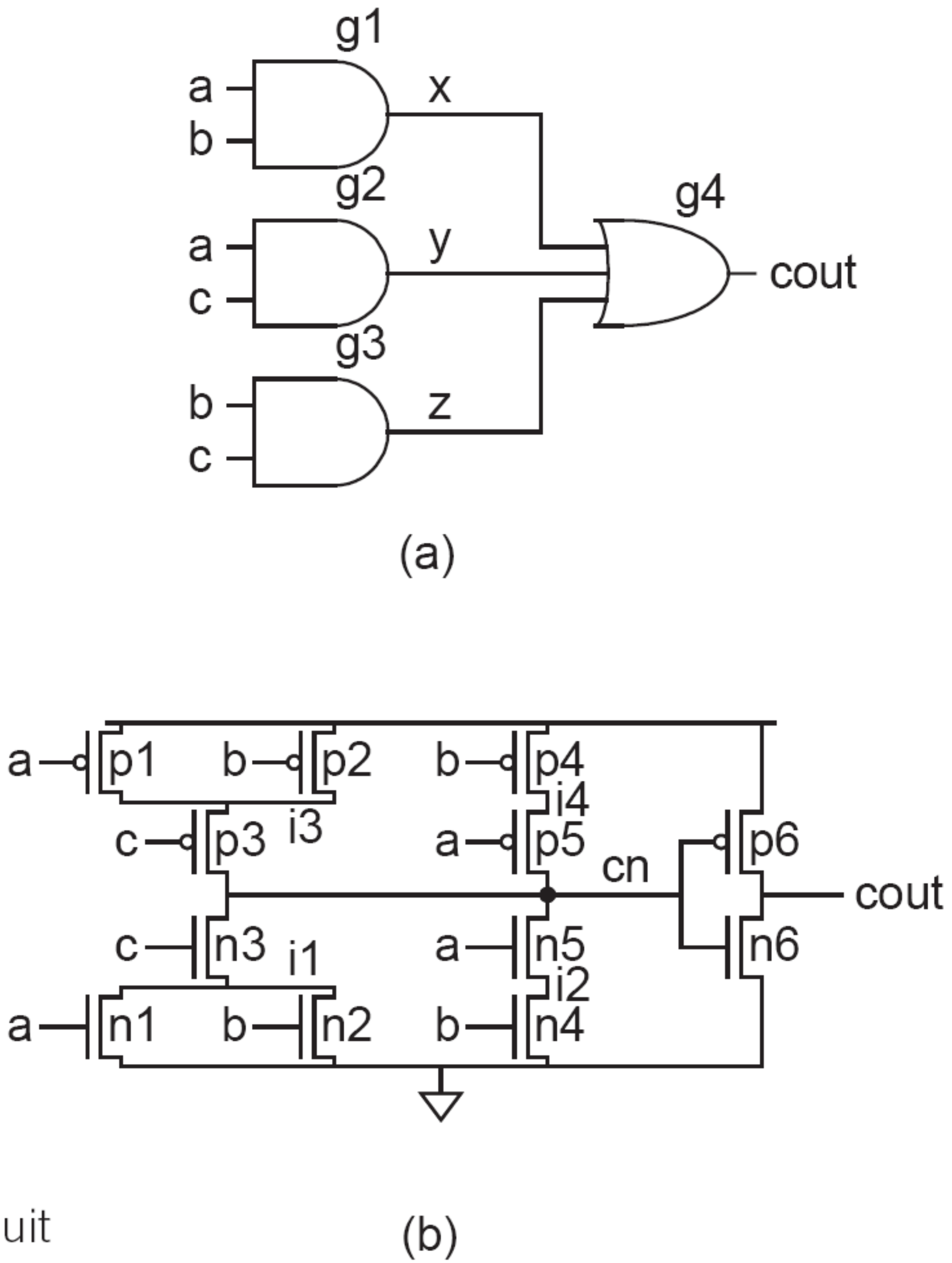


FIGURE 1.61 Carry subcircuit

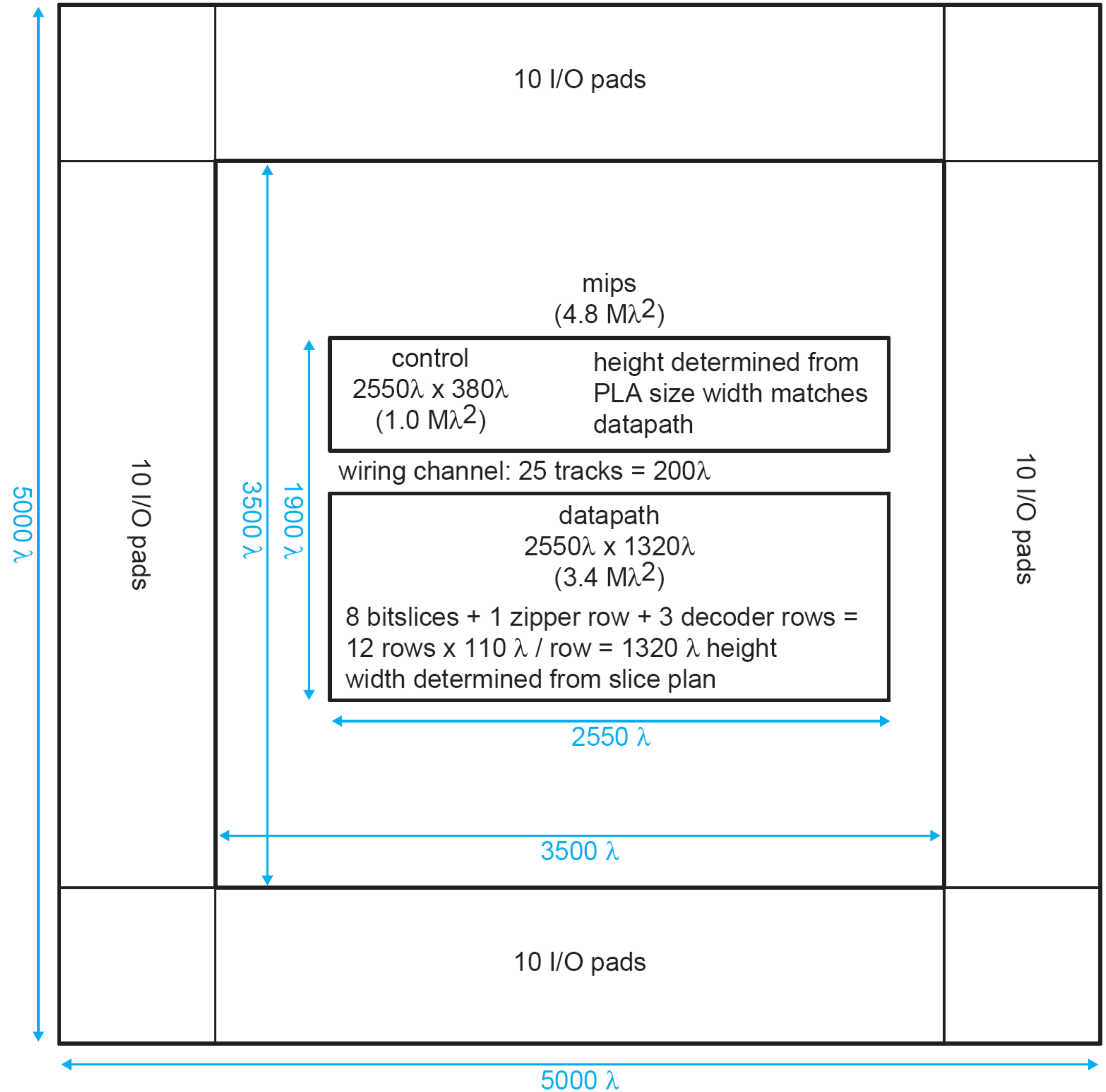


FIGURE 1.62 MIPS floorplan

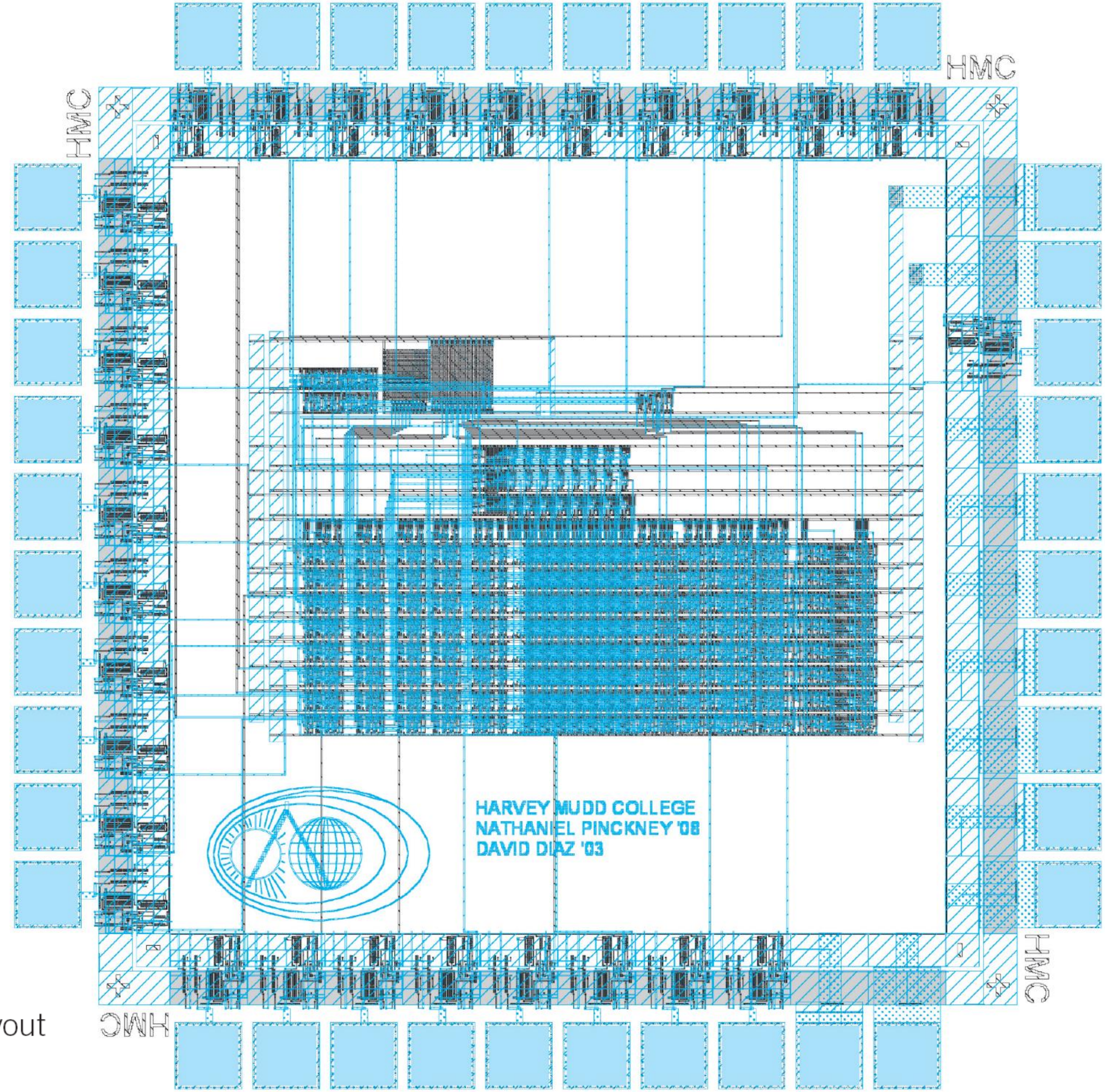


FIGURE 1.63 MIPS layout

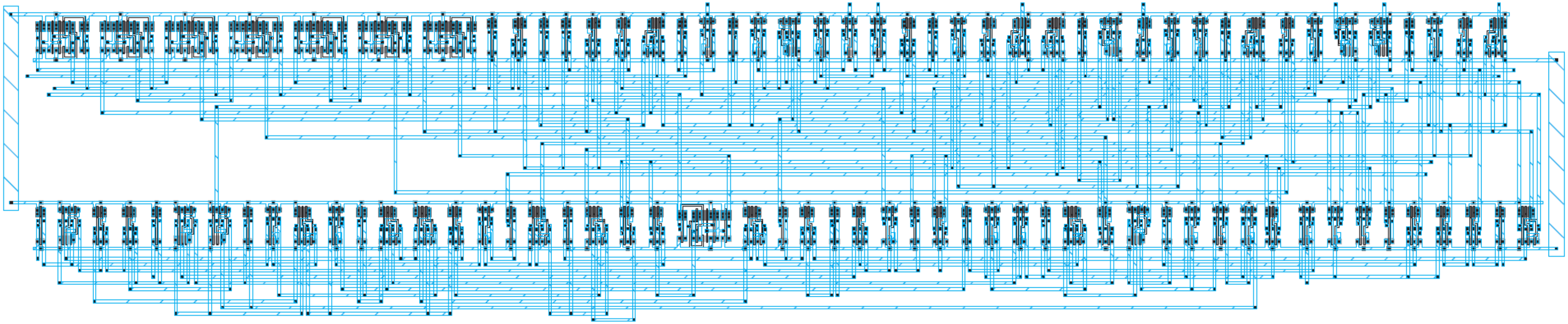


FIGURE 1.64 MIPS controller layout (synthesized)

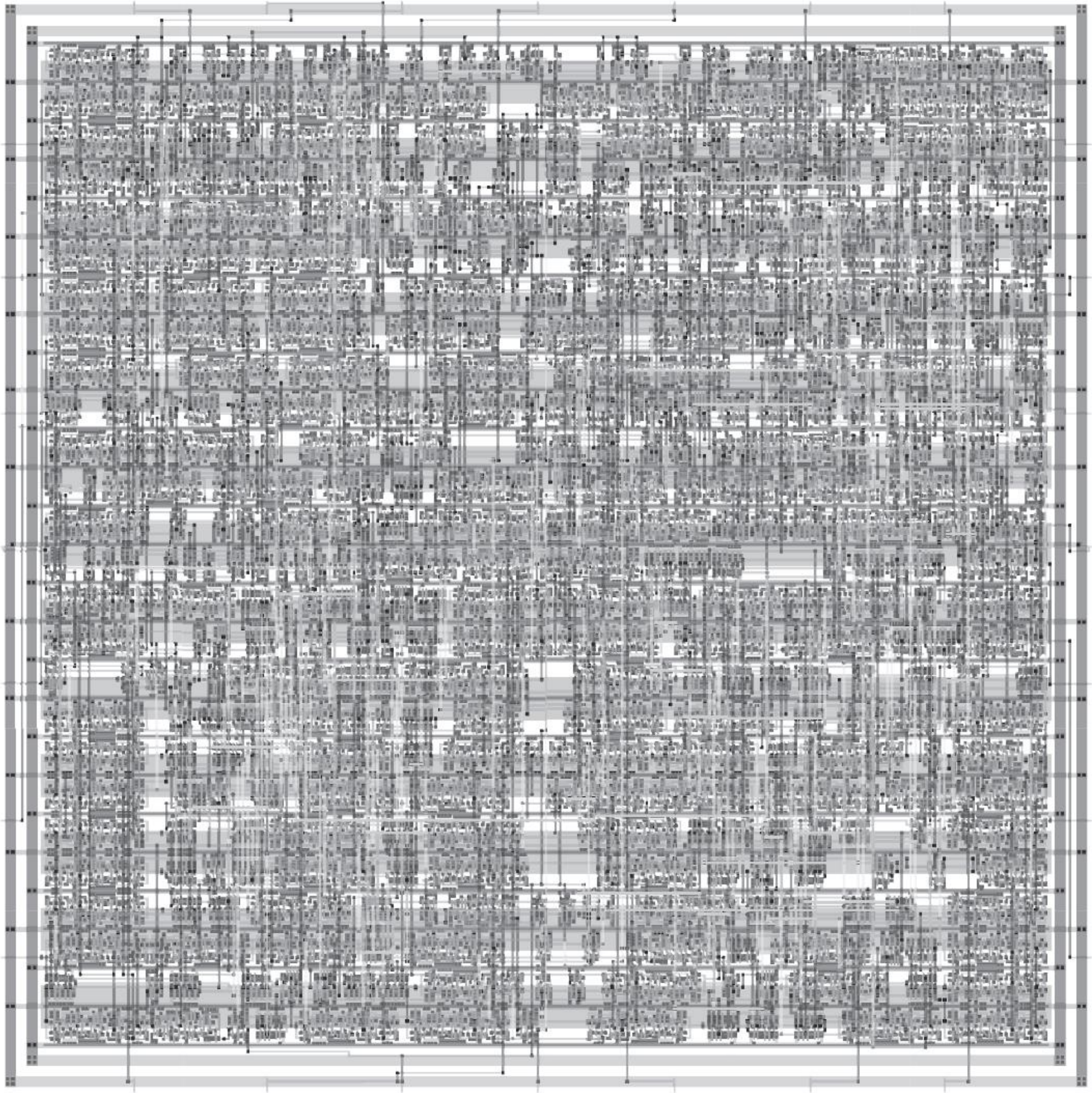


FIGURE 1.65 Synthesized MIPS processor

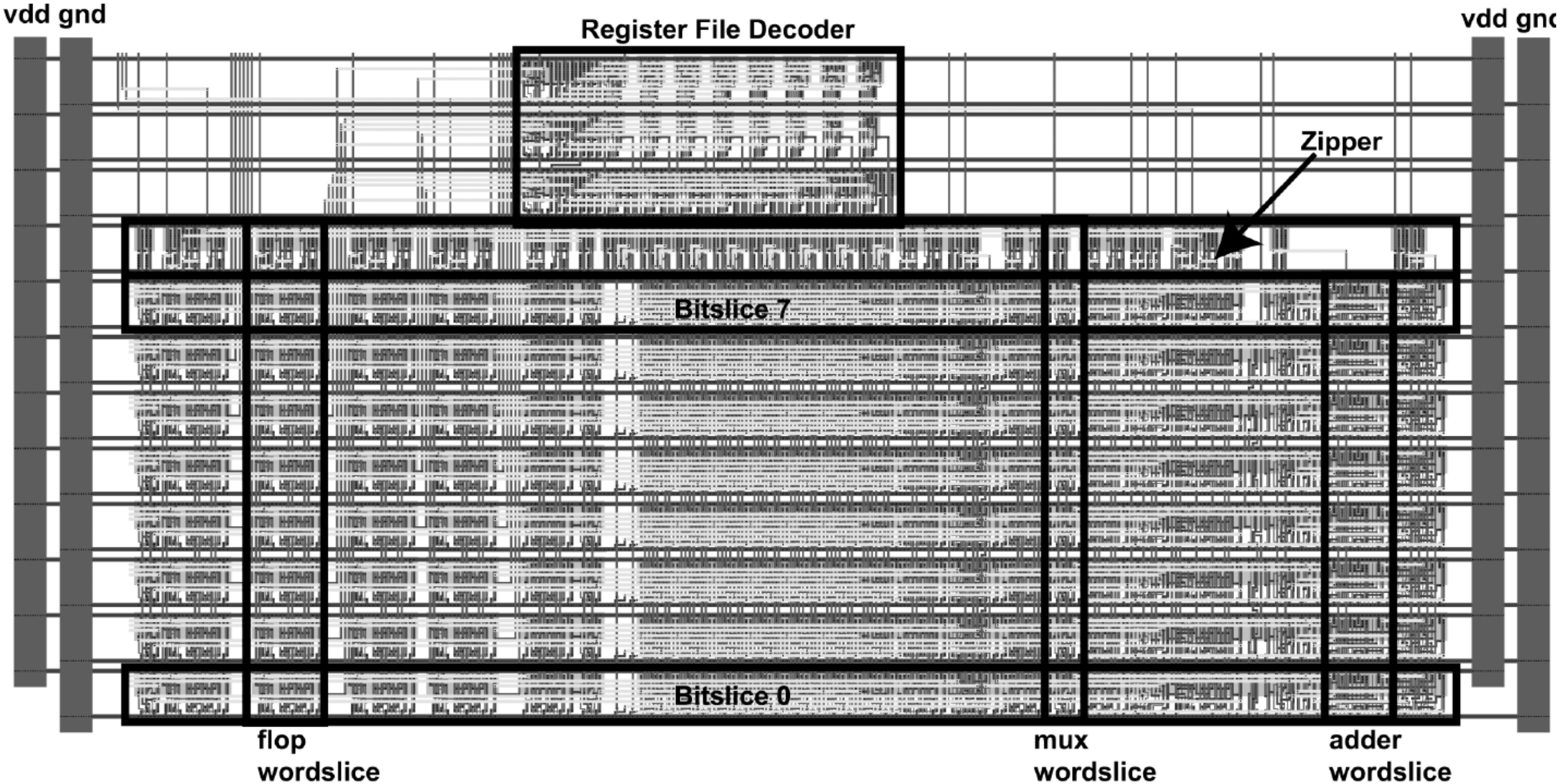


FIGURE 1.67 MIPS datapath layout

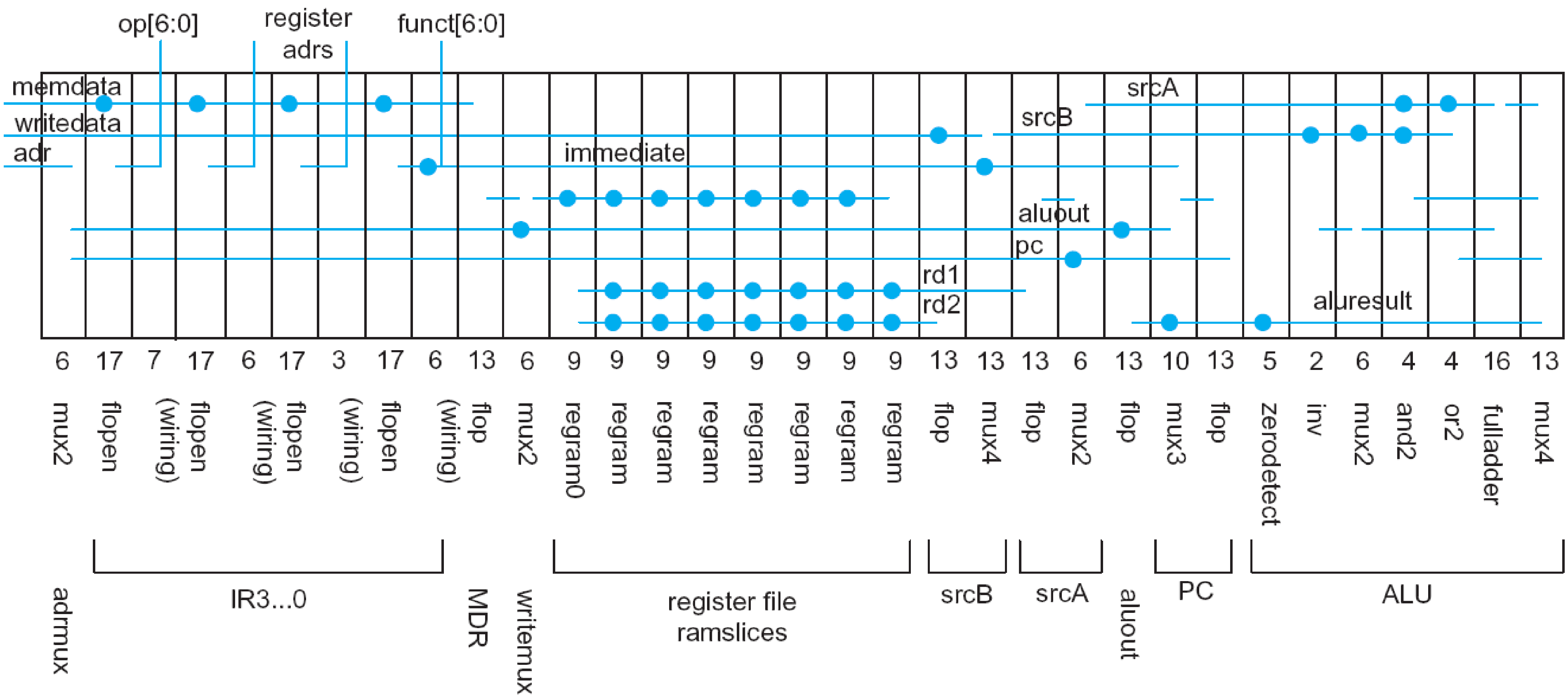


FIGURE 1.68 Datapath slice plan

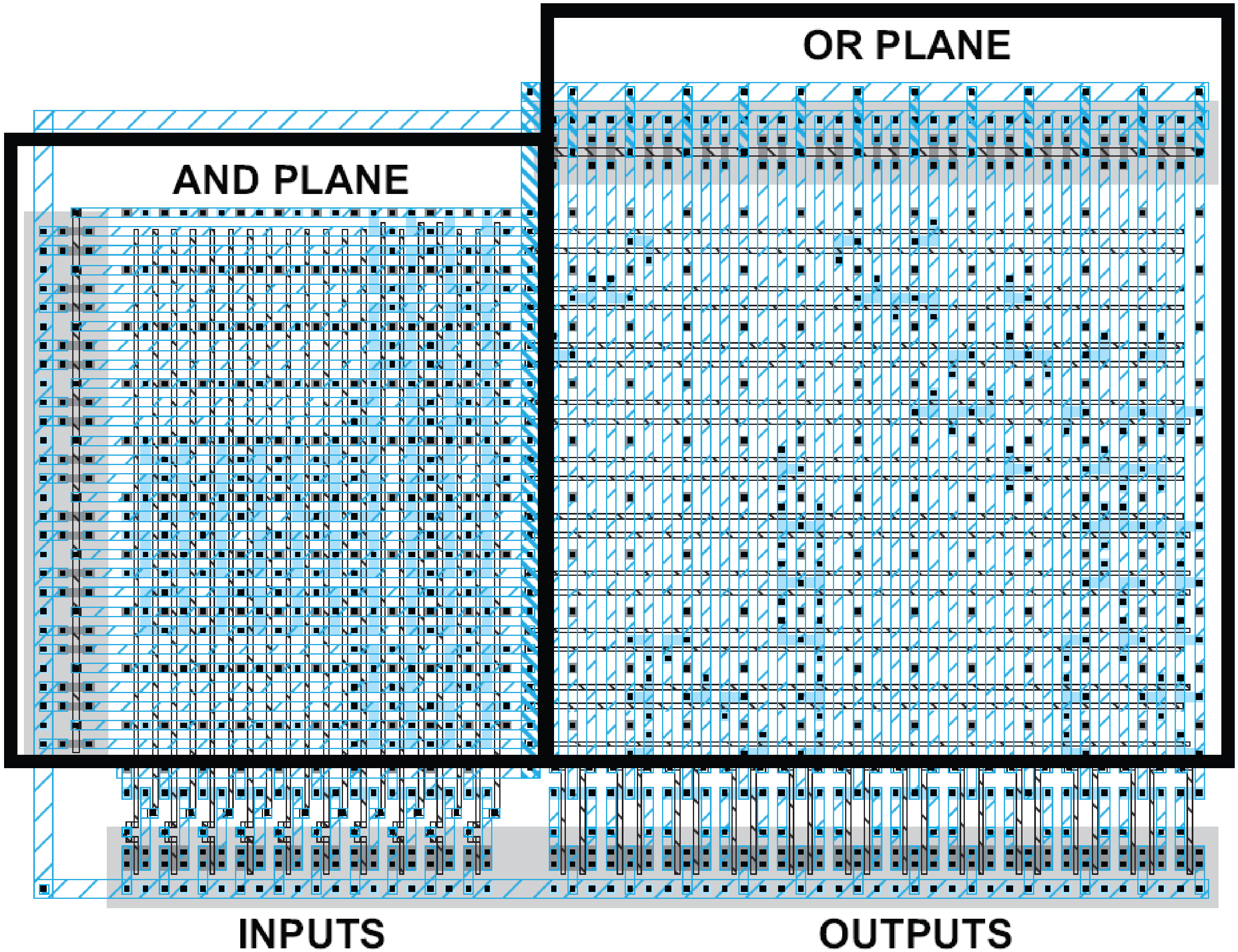


FIGURE 1.69 PLA for control FSM

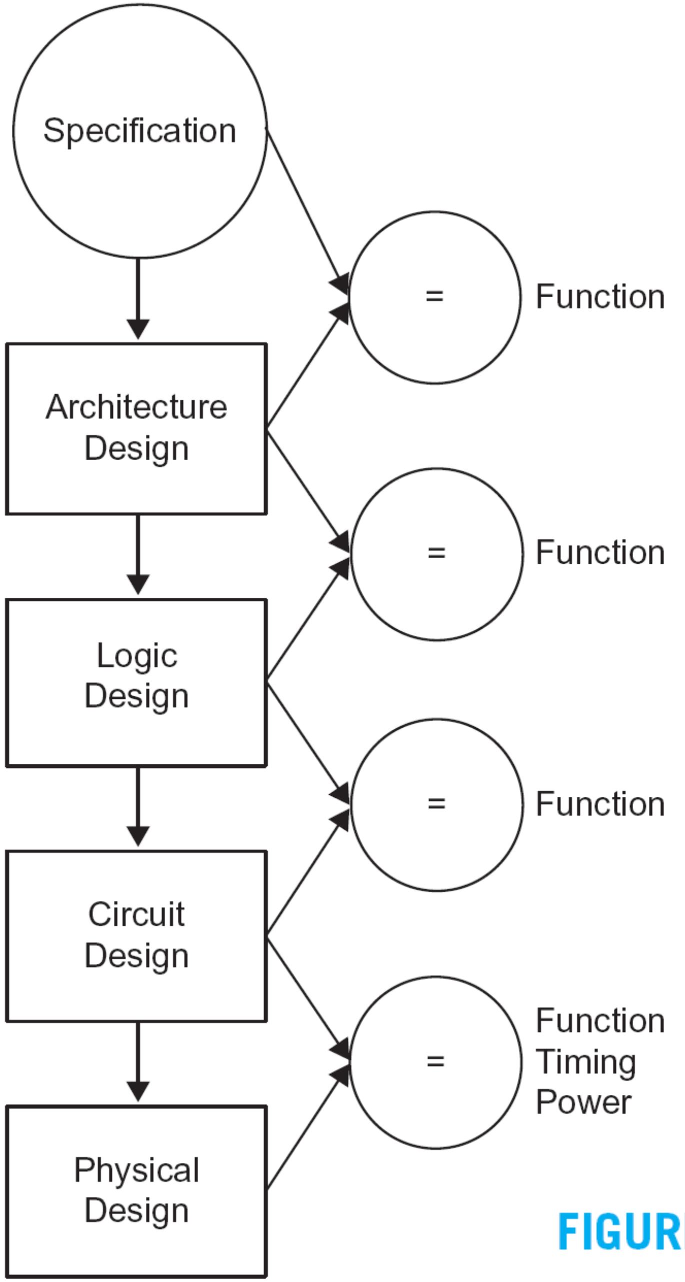


FIGURE 1.70 Design and verification sequence

FIGURE 1.71 Engineer holding processed 12-inch wafer. Photograph courtesy of the Intel Corporation.

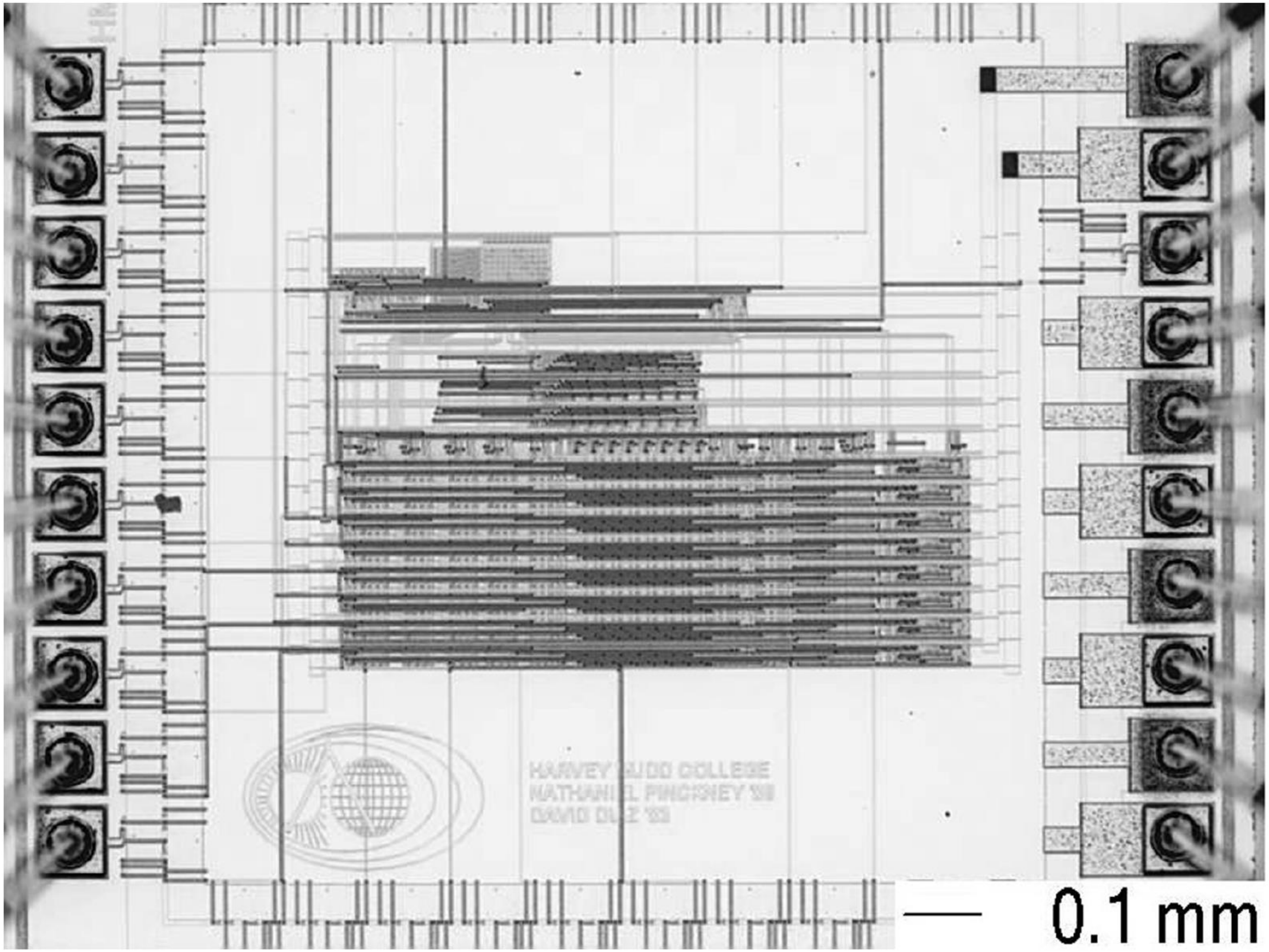


FIGURE 1.72 MIPS processor photomicrograph (only part of pad frame shown)

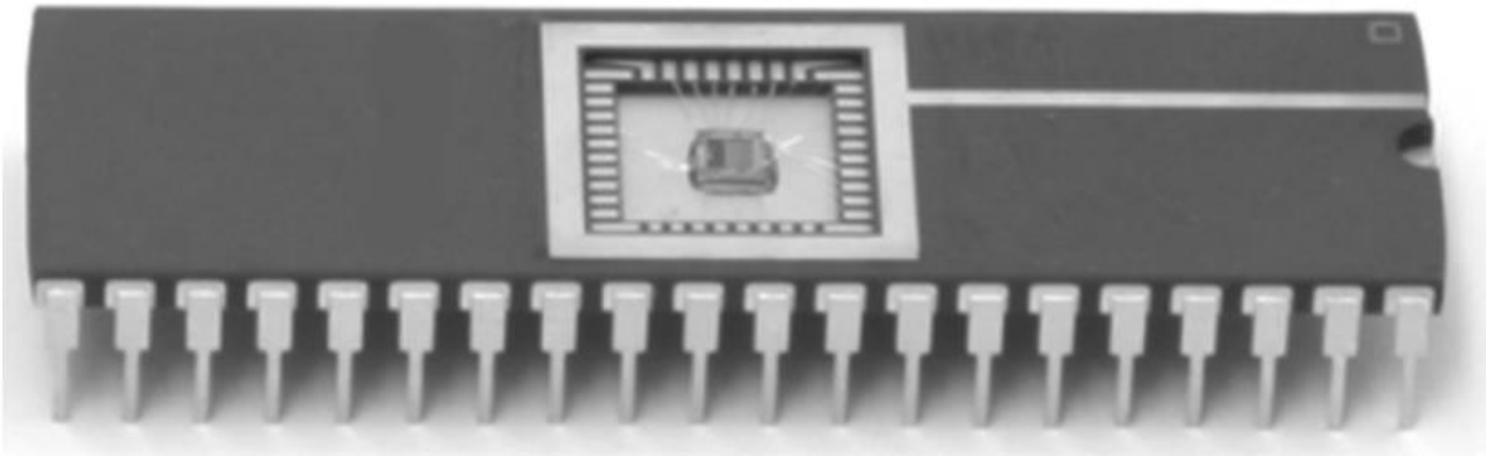


FIGURE 1.73 Chip in a 40-pin dual-inline package

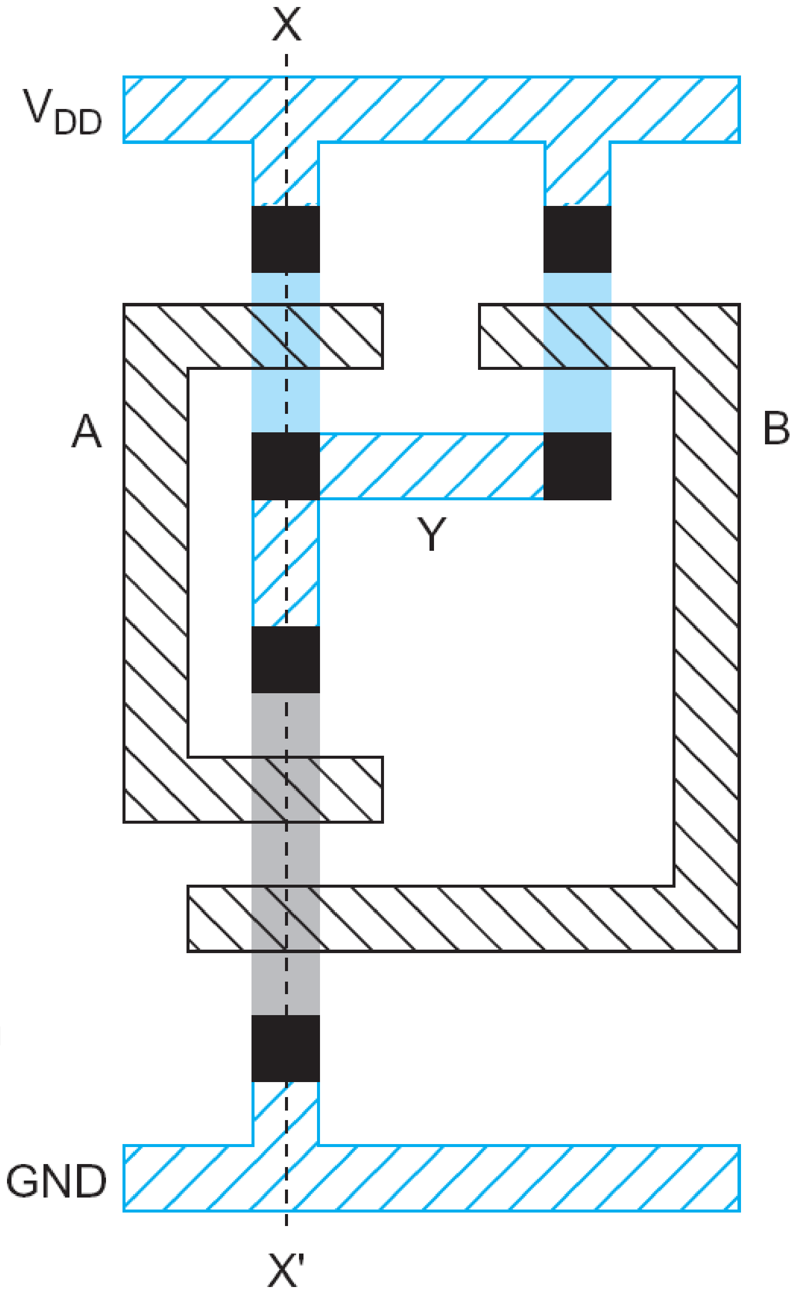


FIGURE 1.74 2-input NAND gate stick diagram

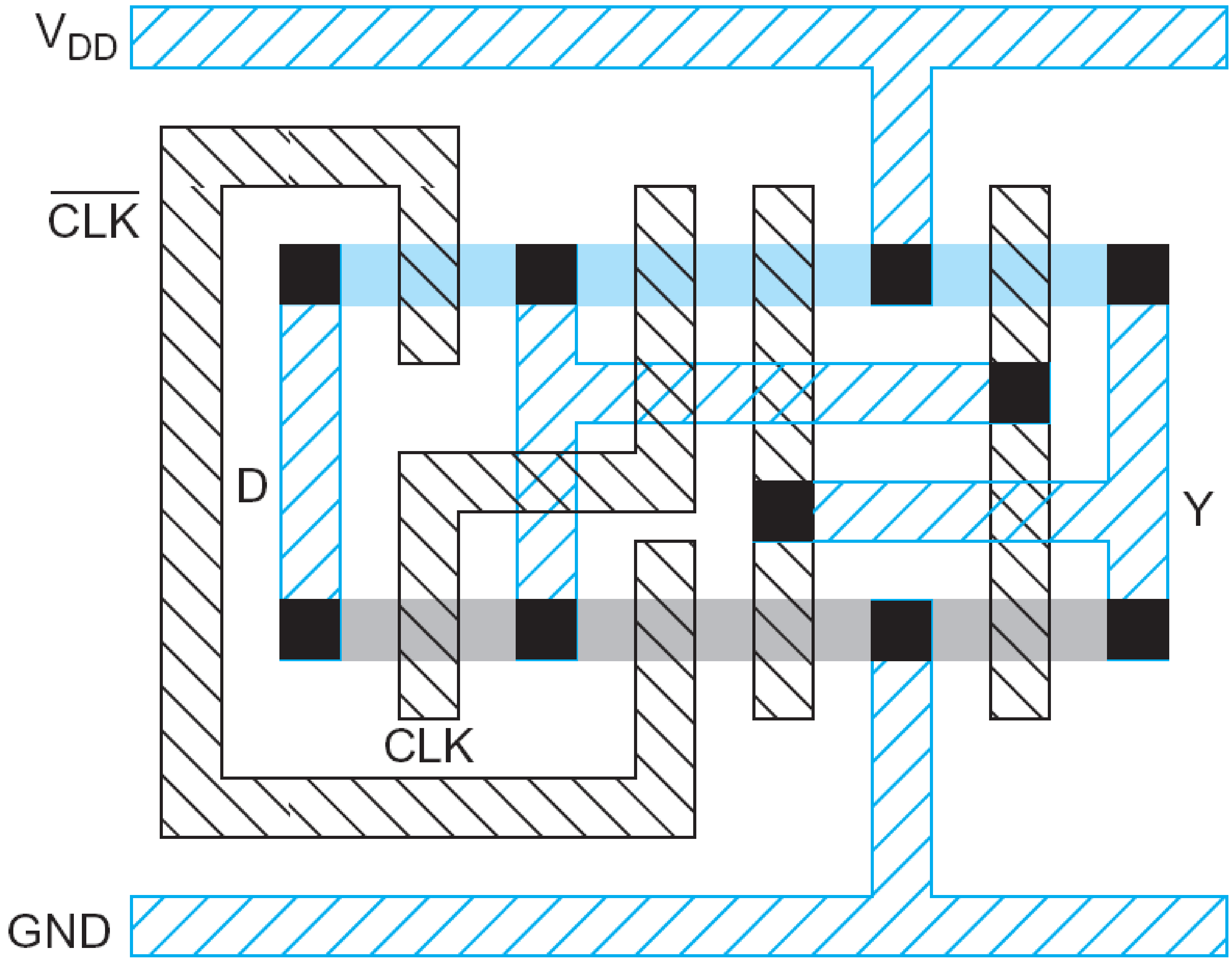


FIGURE 1.75 Level-sensitive latch stick diagram