Digital Integrated Circuits

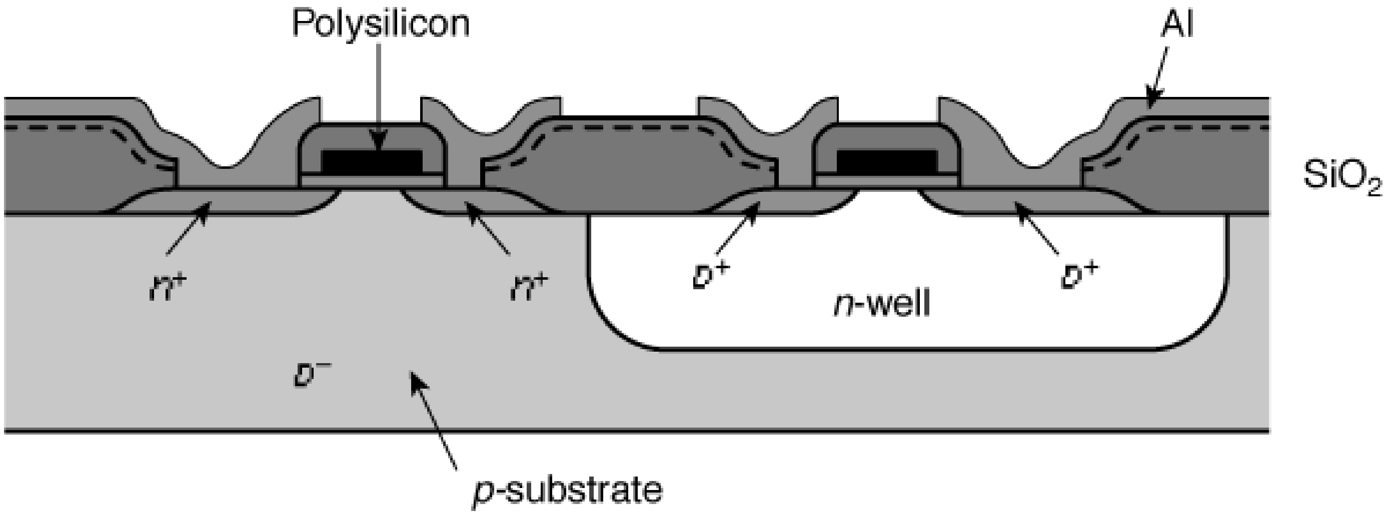
A Design Perspective

Jan M. Rabaey
Anantha Chandrakasan
Borivoje Nikolic

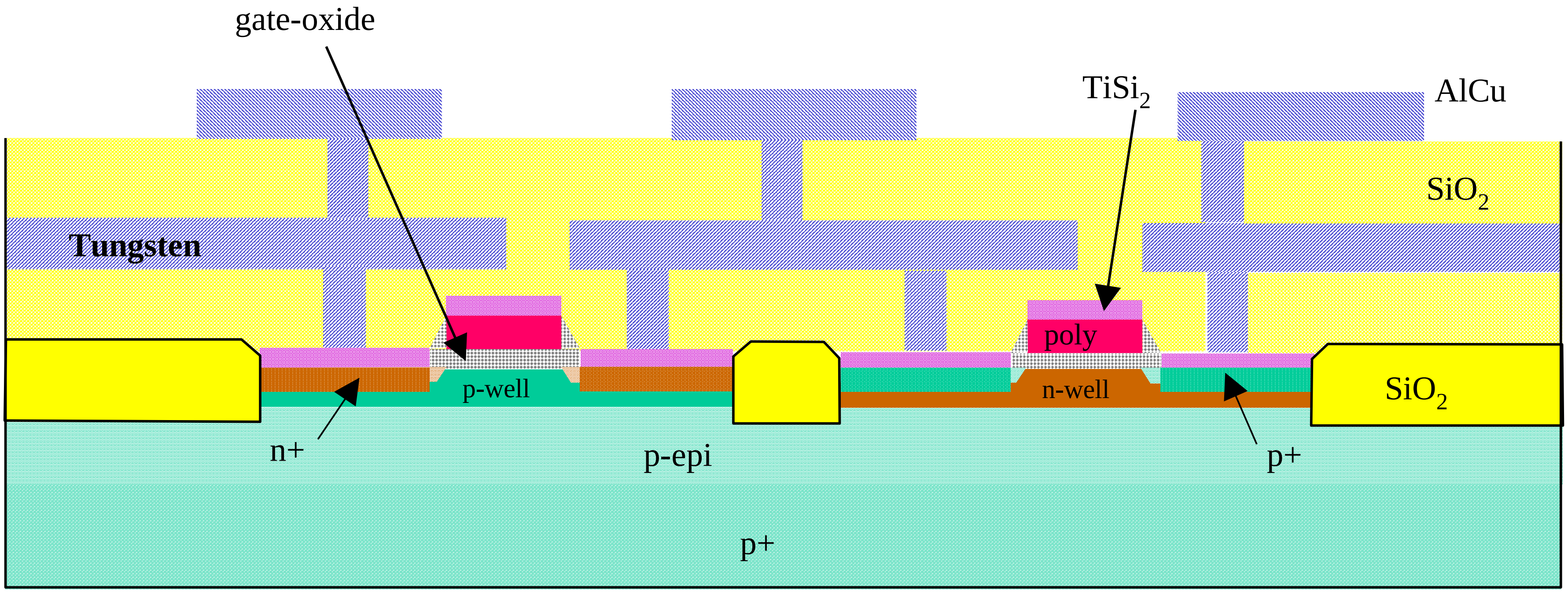
Manufacturing Process

July 30, 2002

CMOS Process

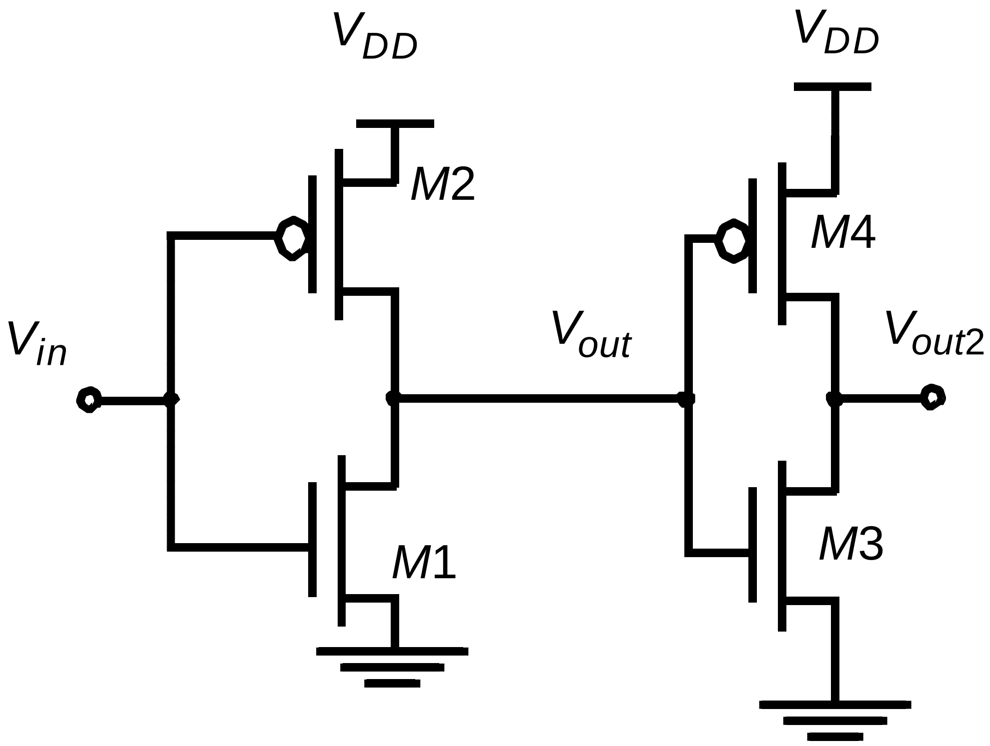


A Modern CMOS Process

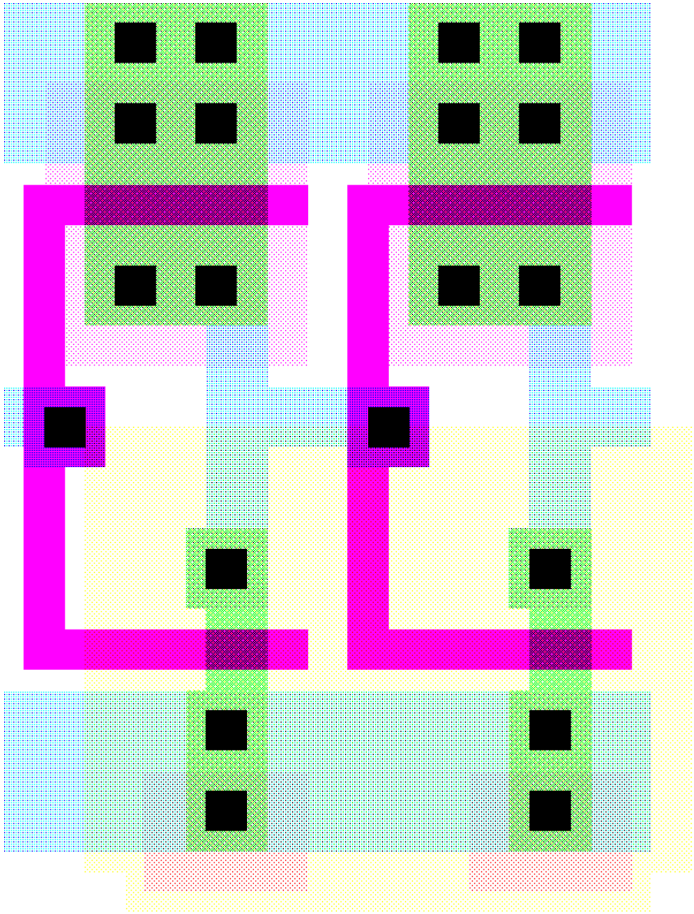


Dual-Well Trench-Isolated CMOS Process

Circuit Under Design



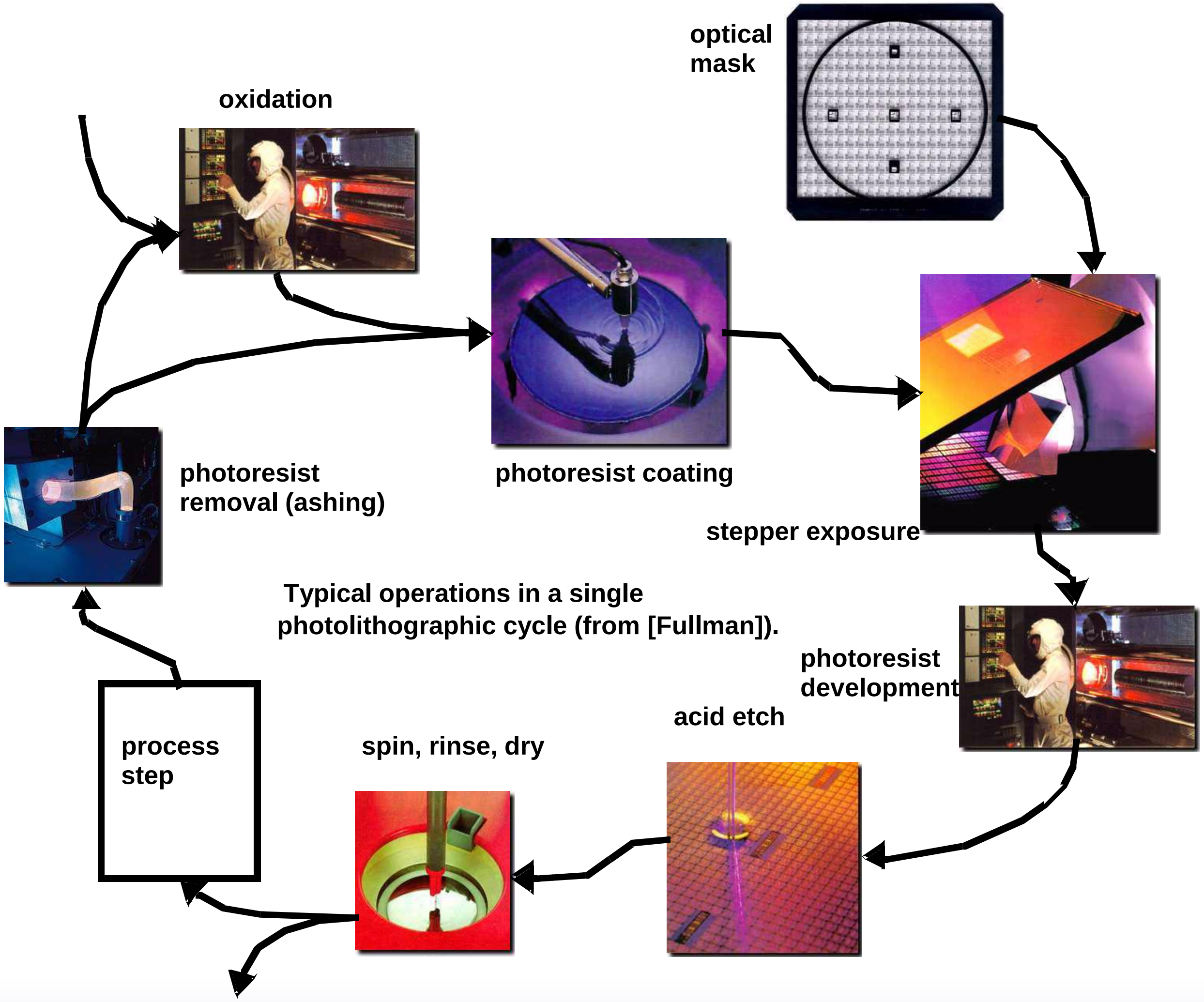
Its Layout View



The Manufacturing Process

For a great tour through the IC manufacturing process and its different steps, check http://www.fullman.com/semiconductors/semiconductors.html

Photo-Lithographic Process



optical mask

oxidation

photoresist coating

stepper exposure

photoresist development

acid etch

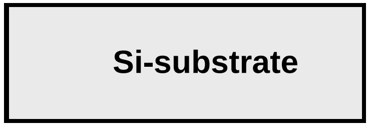
spin, rinse, dry

process step

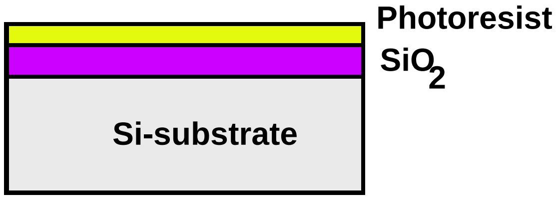
photoresist removal (ashing)

Typical operations in a single photolithographic cycle (from [Fullman]).

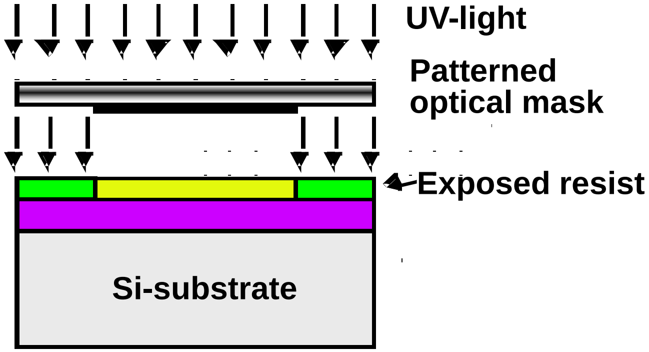
Patterning of SiO2



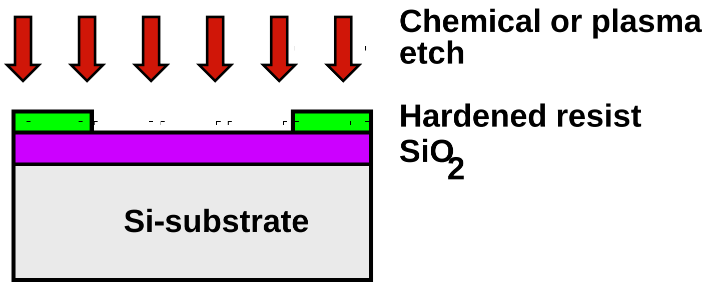
(a) Silicon base material



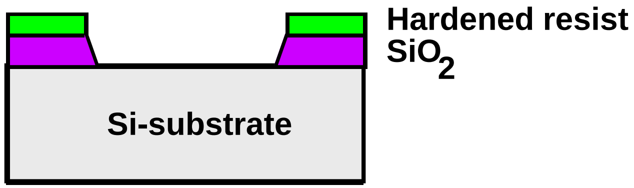
(b) After oxidation and deposition of negative photoresist



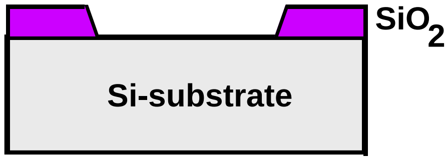
(c) Stepper exposure



(d) After development and etching of resist, chemical or plasma etch of SiO_2



(e) After etching



(f) Final result after removal of resist

CMOS Process at a Glance

Define active areas
Etch and fill trenches

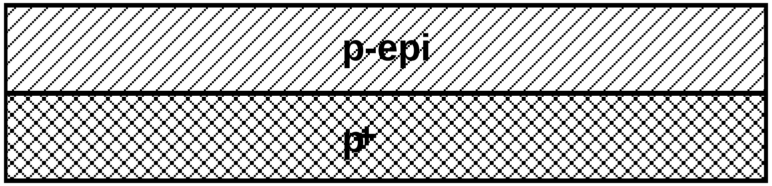
Implant well regions

Deposit and pattern polysilicon layer

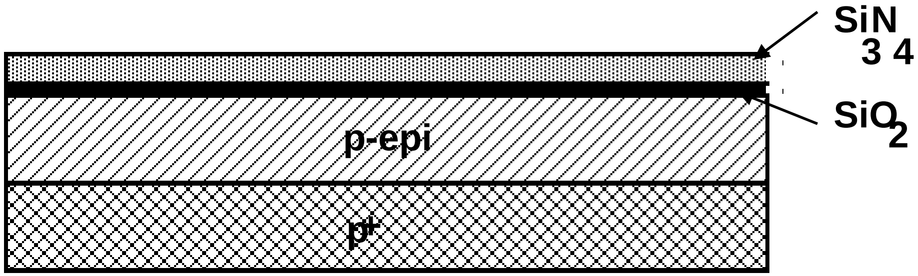
Implant source and drain regions and substrate contacts

Create contact and via windows
Deposit and pattern metal layers

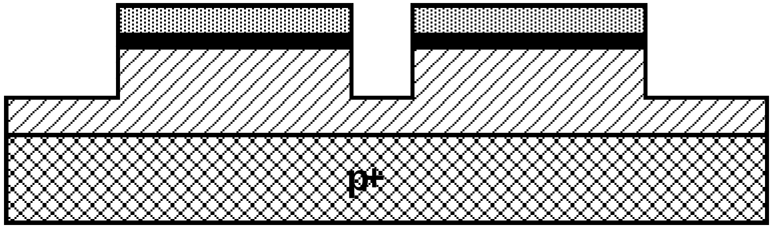
CMOS Process Walk-Through



(a) Base material: p+ substrate with p-epi layer

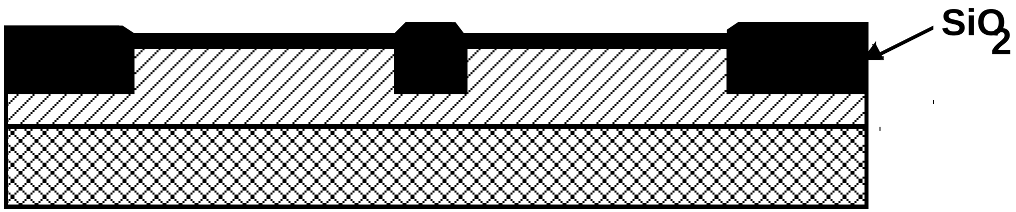


(b) After deposition of gate-oxide and sacrificial nitride (acts as a buffer layer)

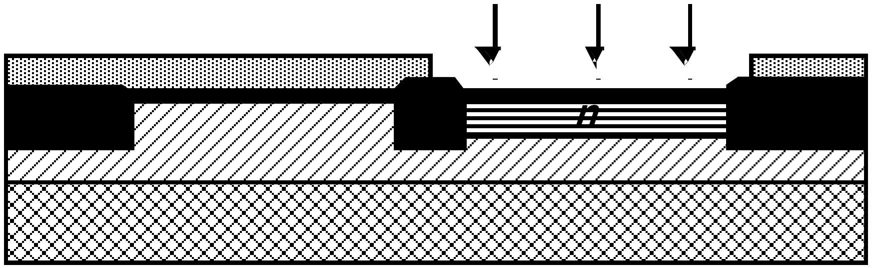


(c) After plasma etch of insulating trenches using the inverse of the active area mask

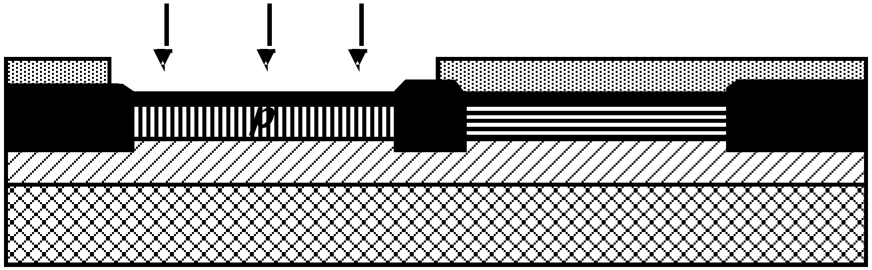
CMOS Process Walk-Through



(d) After trench filling, CMP planarization, and removal of sacrificial nitride

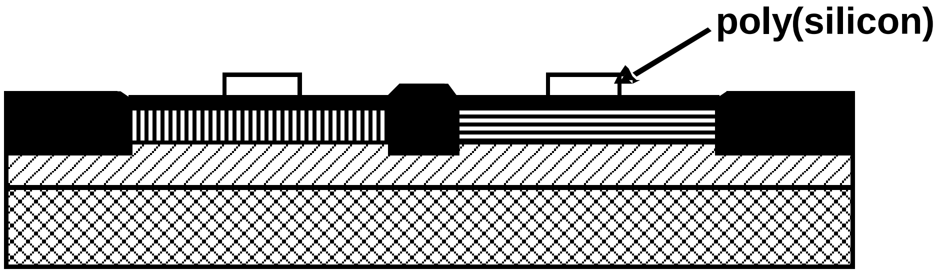


(e) After n-well and V_{Tp} adjust implants

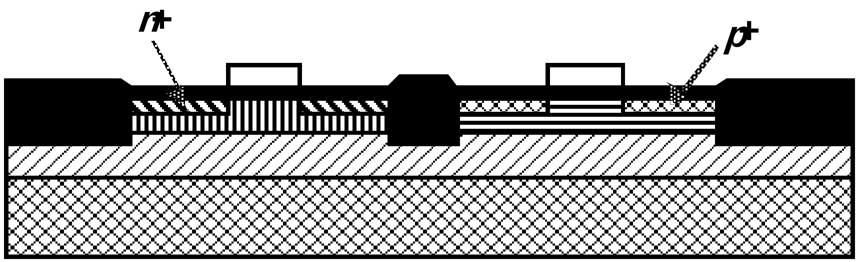


(f) After p-well and V_{Tn} adjust implants

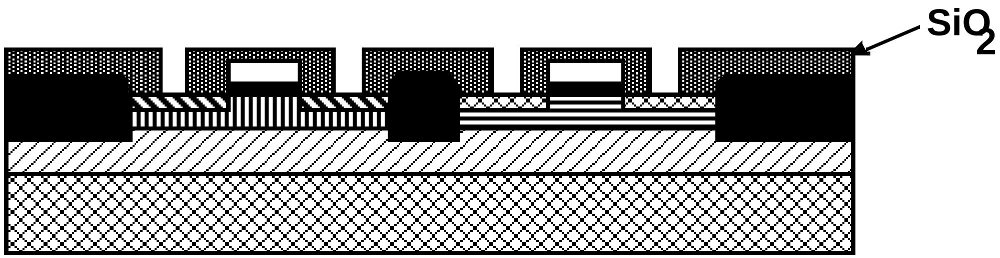
CMOS Process Walk-Through



(g) After polysilicon deposition and etch

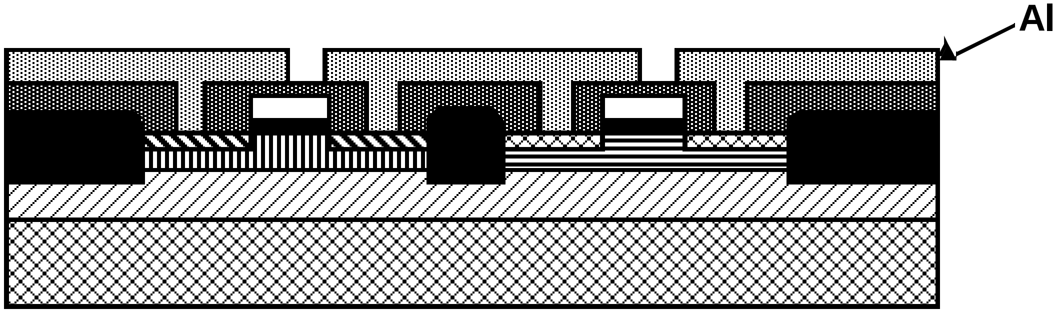


(h) After *n*+ source/drain and *p*+ source/drain implants. These steps also dope the polysilicon.

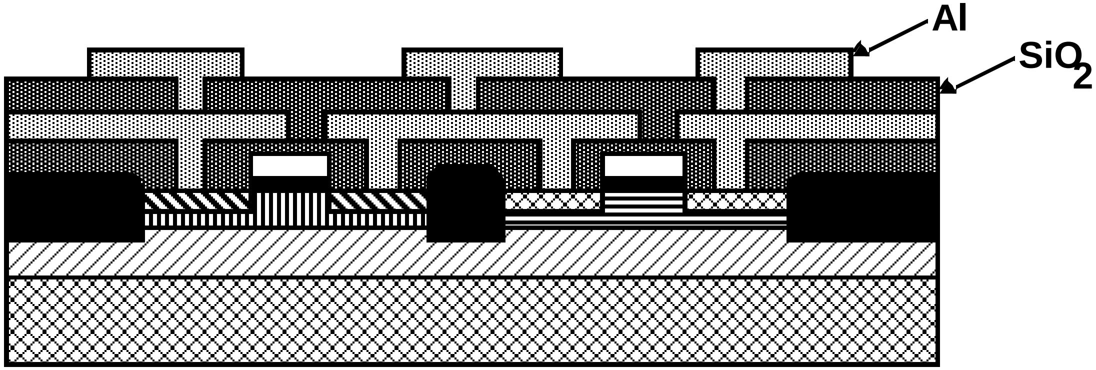


(i) After deposition of SiO_2 insulator and contact hole etch.

CMOS Process Walk-Through

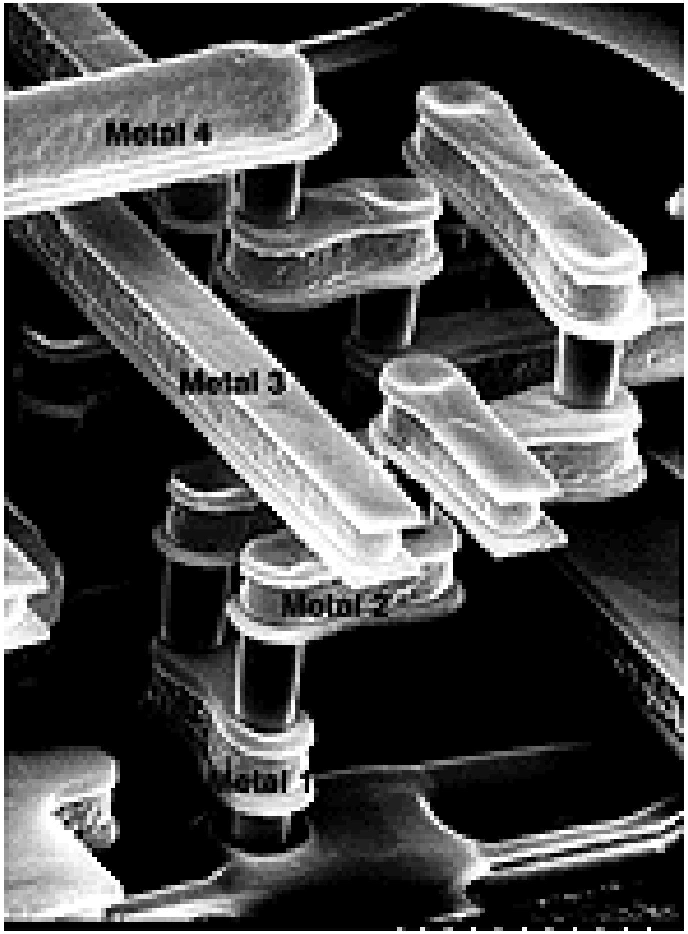


(j) After deposition and patterning of first Al layer.

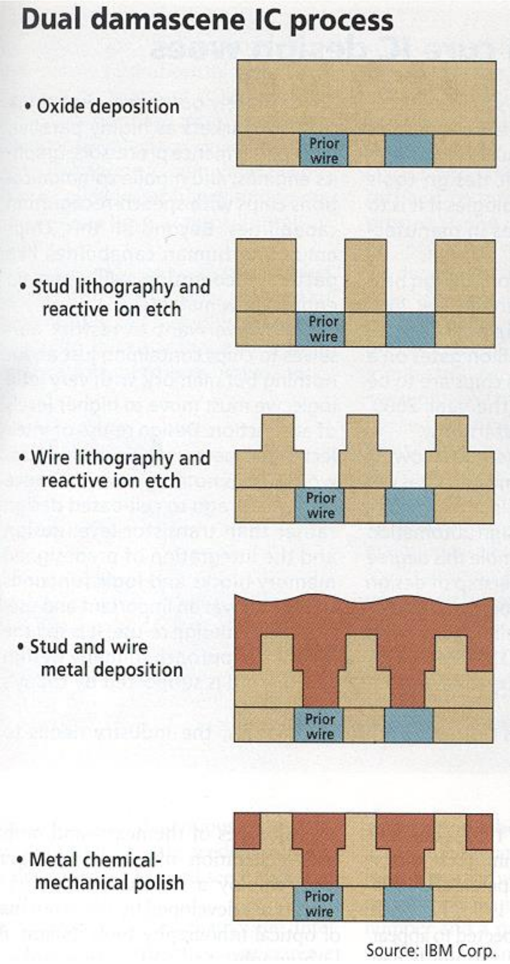


(k) After deposition of SiO$_2$ insulator, etching of via's, deposition and patterning of second layer of Al.

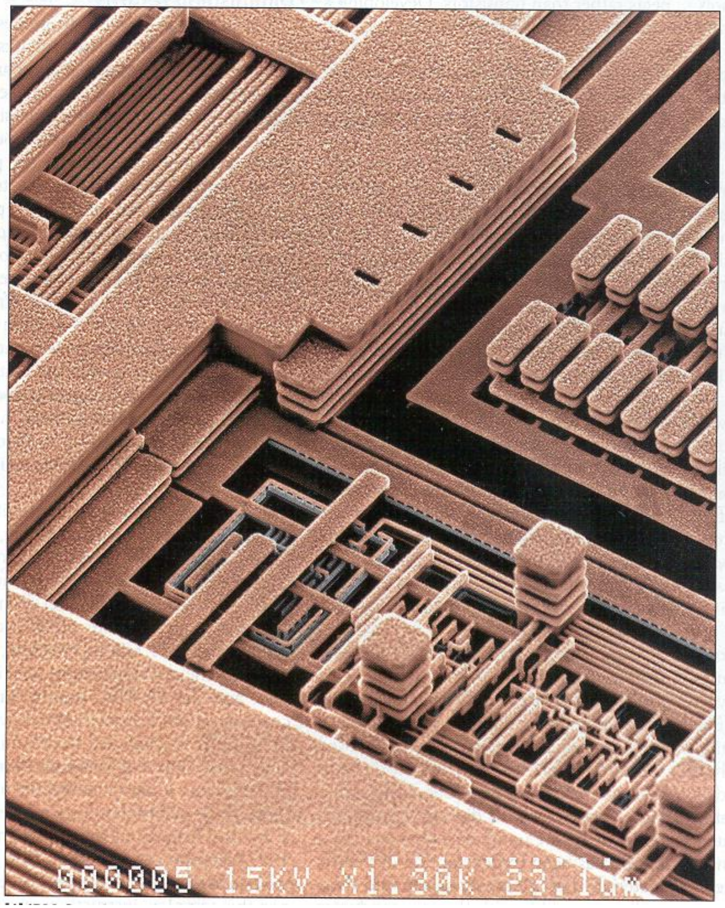
Advanced Metallization



Advanced Metallization

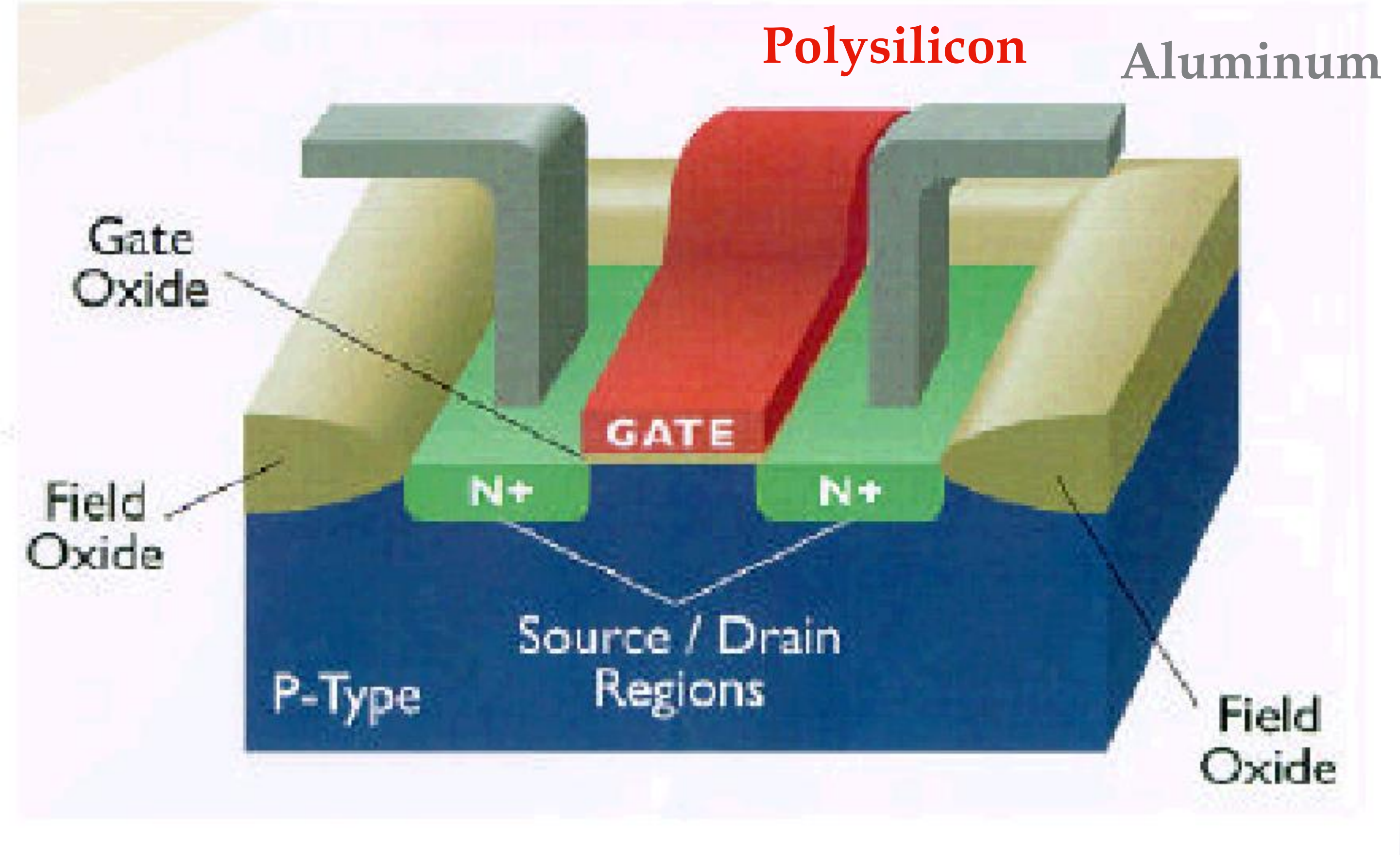


Source: IBM Corp.



Design Rules

3D Perspective



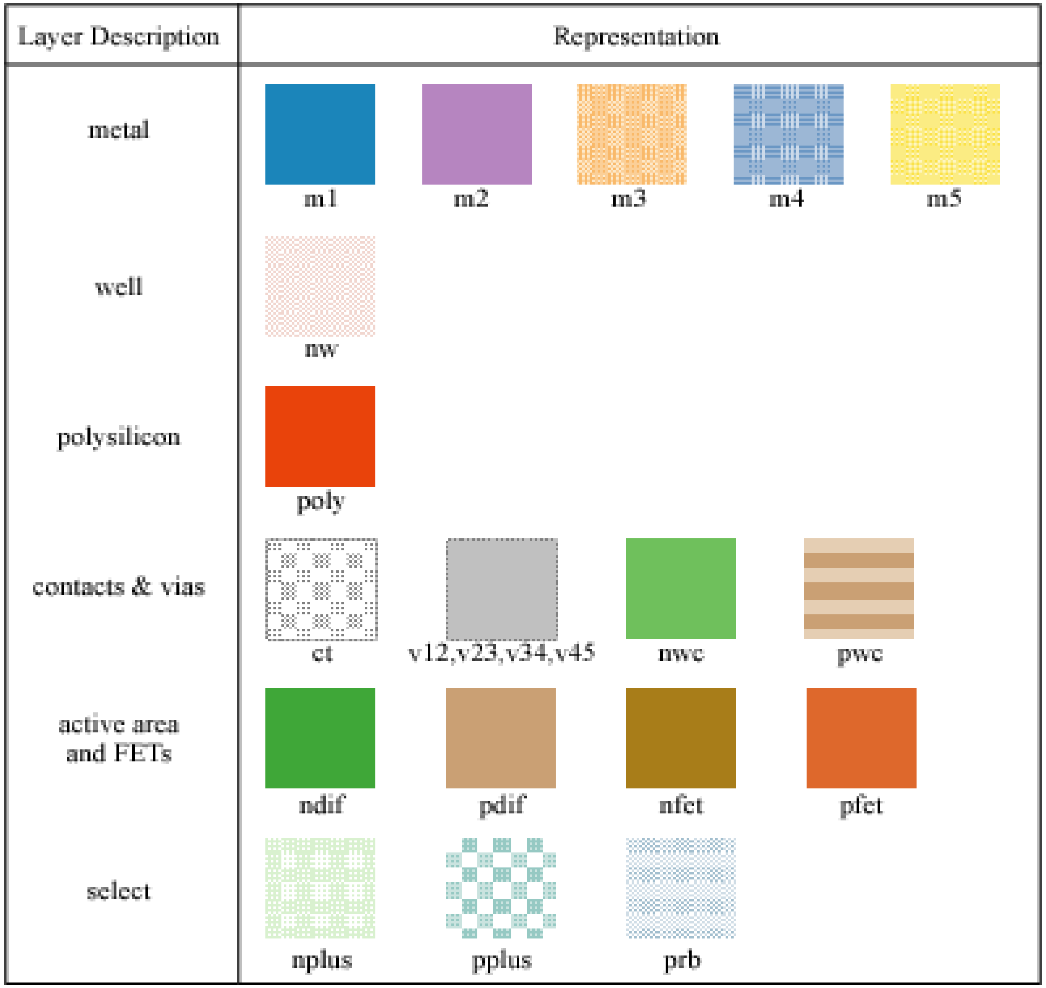
Design Rules

- ❑ Interface between designer and process engineer
- ❑ Guidelines for constructing process masks
- ❑ Unit dimension: Minimum line width
  - scalable design rules: lambda parameter
  - absolute dimensions (micron rules)

CMOS Process Layers

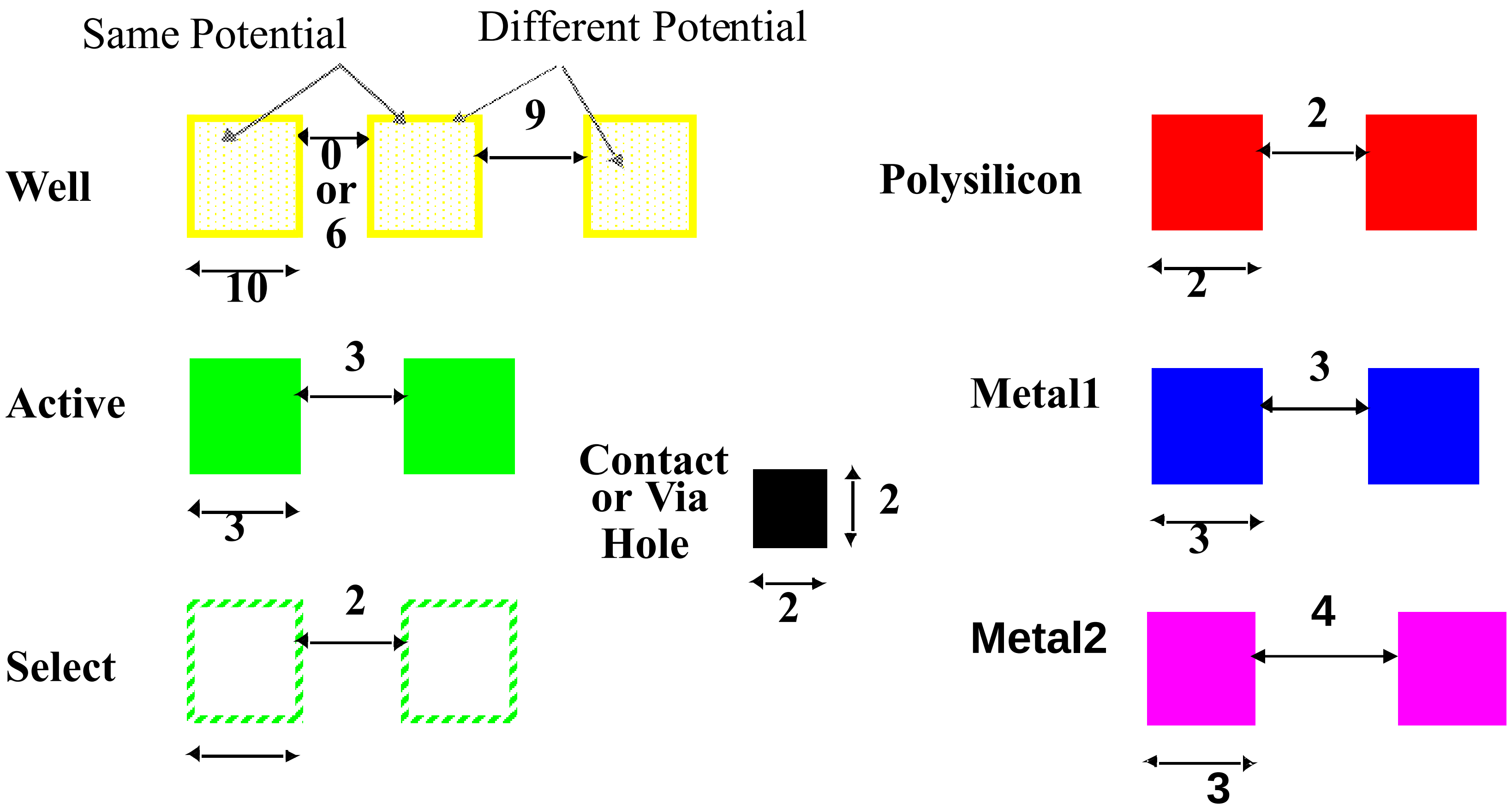
Layer	Color	Representation
Well (p,n)	Yellow	🟨
Active Area (n+,p+)	Green	🟩
Select (p+,n+)	Green	⬚
Polysilicon	Red	🟥
Metal1	Blue	🟦
Metal2	Magenta	🟪
Contact To Poly	Black	⬛
Contact To Diffusion	Black	⬛
Via	Black	⬛

Layers in 0.25 μm CMOS process

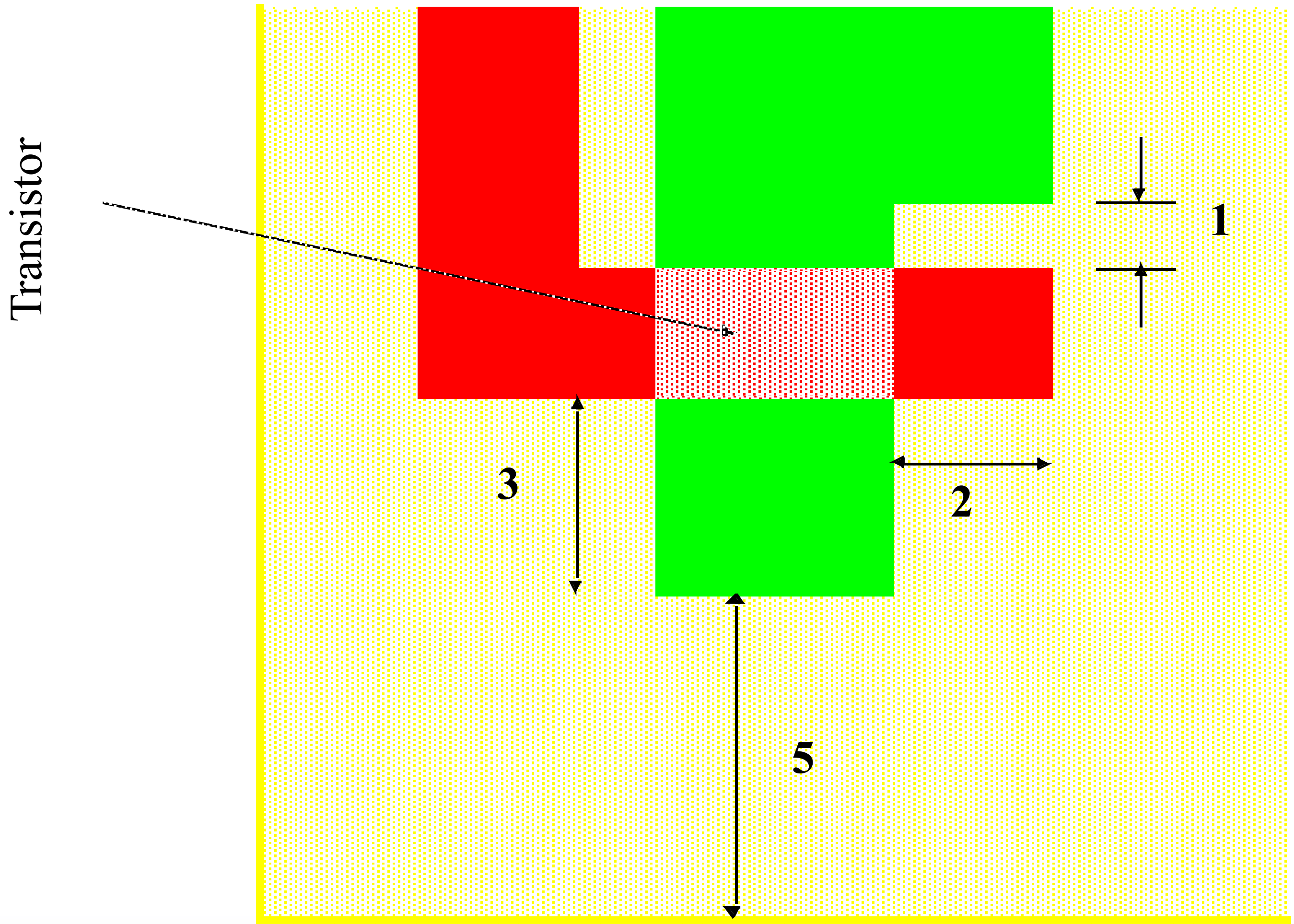


Layer Description	Representation				
metal	m1	m2	m3	m4	m5
well	nw				
polysilicon	poly				
contacts & vias	ct	v12,v23,v34,v45	nwc	pwc	
active area and FETs	ndif	pdif	nfet	pfet	
select	nplus	pplus	prb		

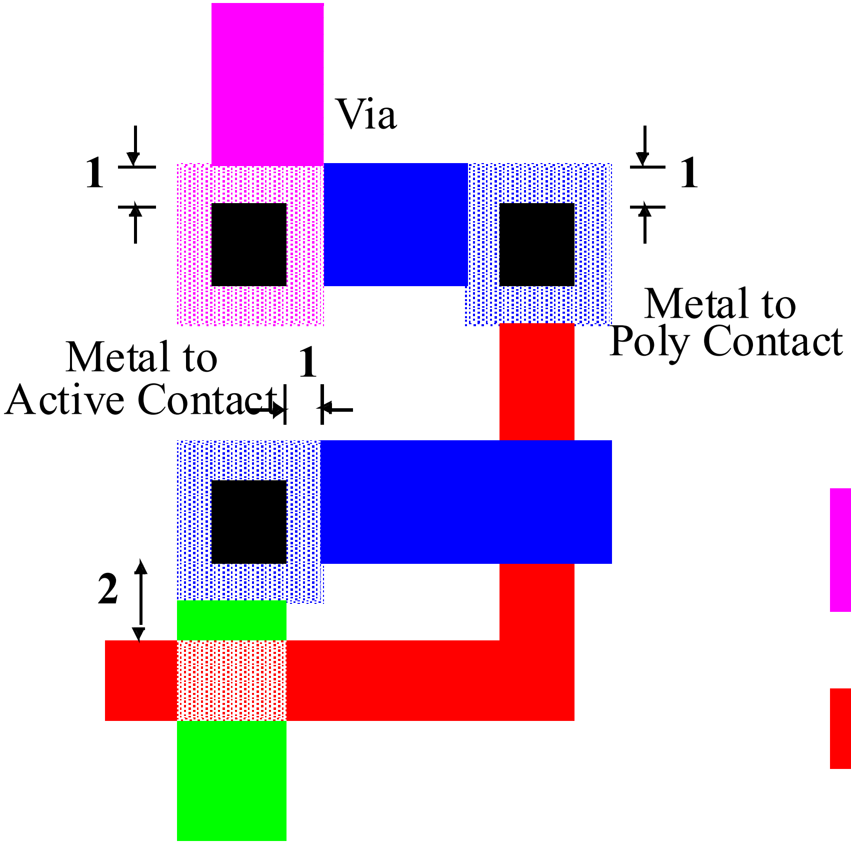
Intra-Layer Design Rules

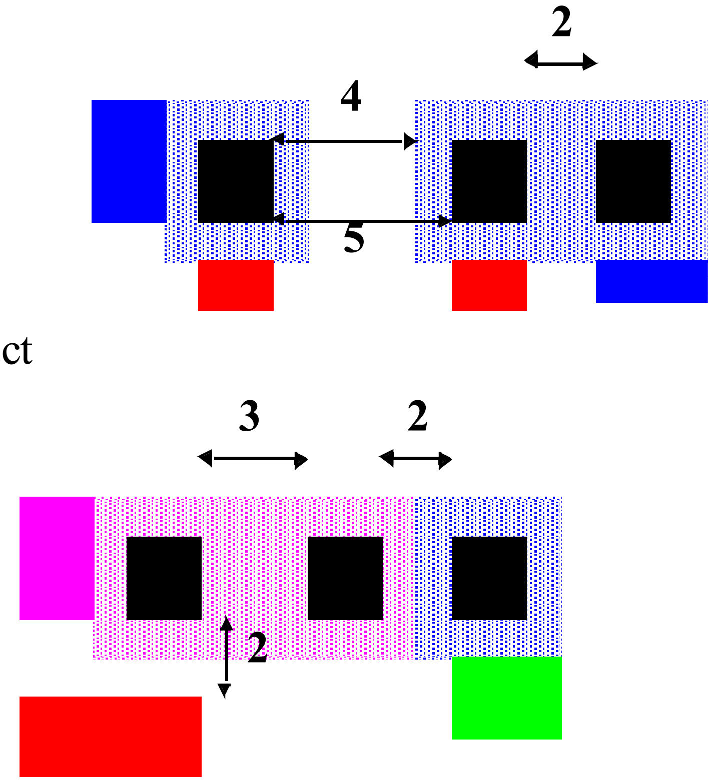


Transistor Layout

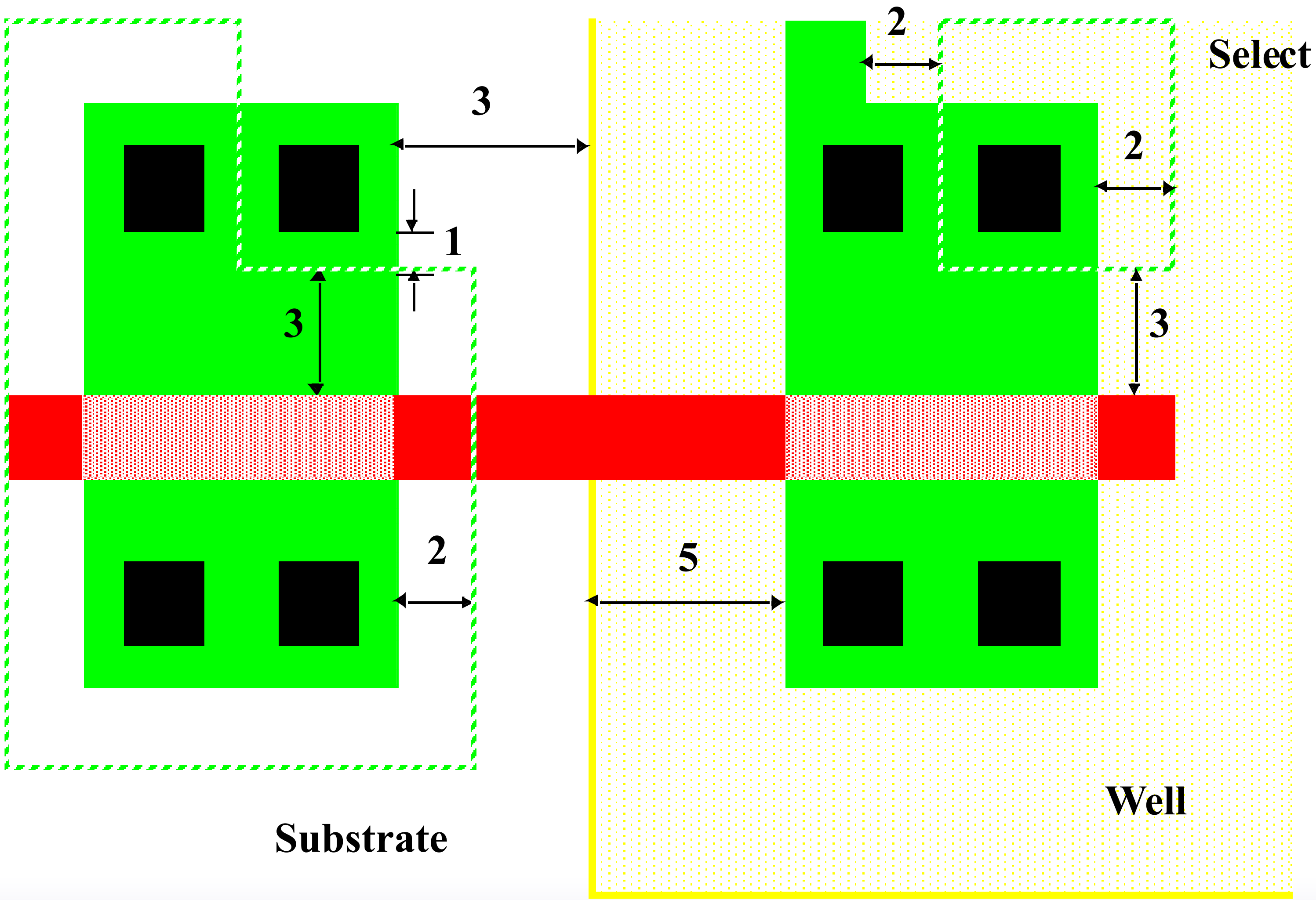


Vias and Contacts

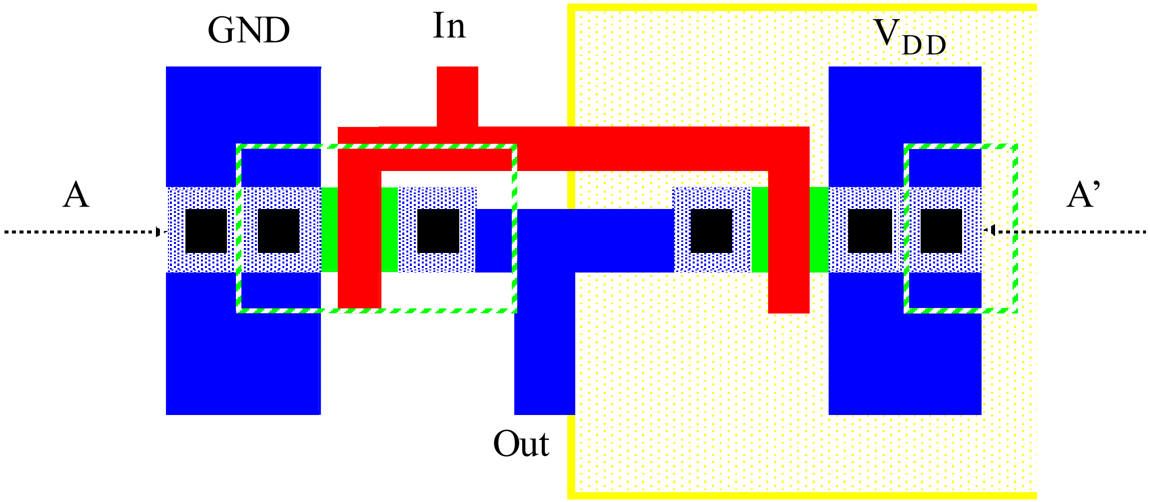




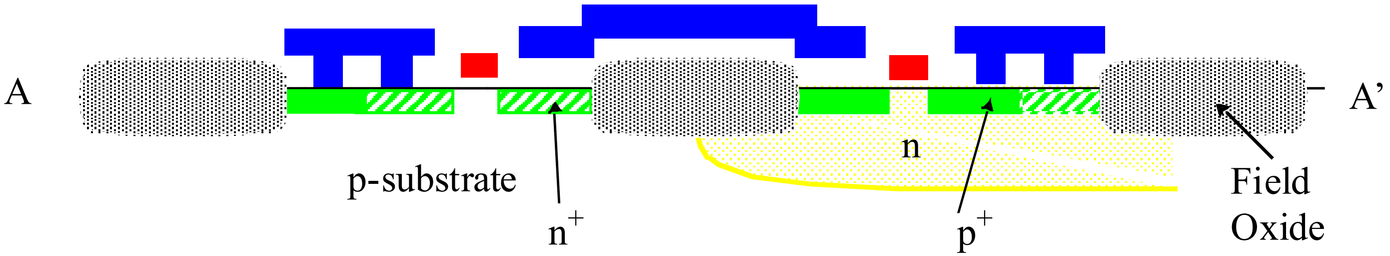
Select Layer



CMOS Inverter Layout

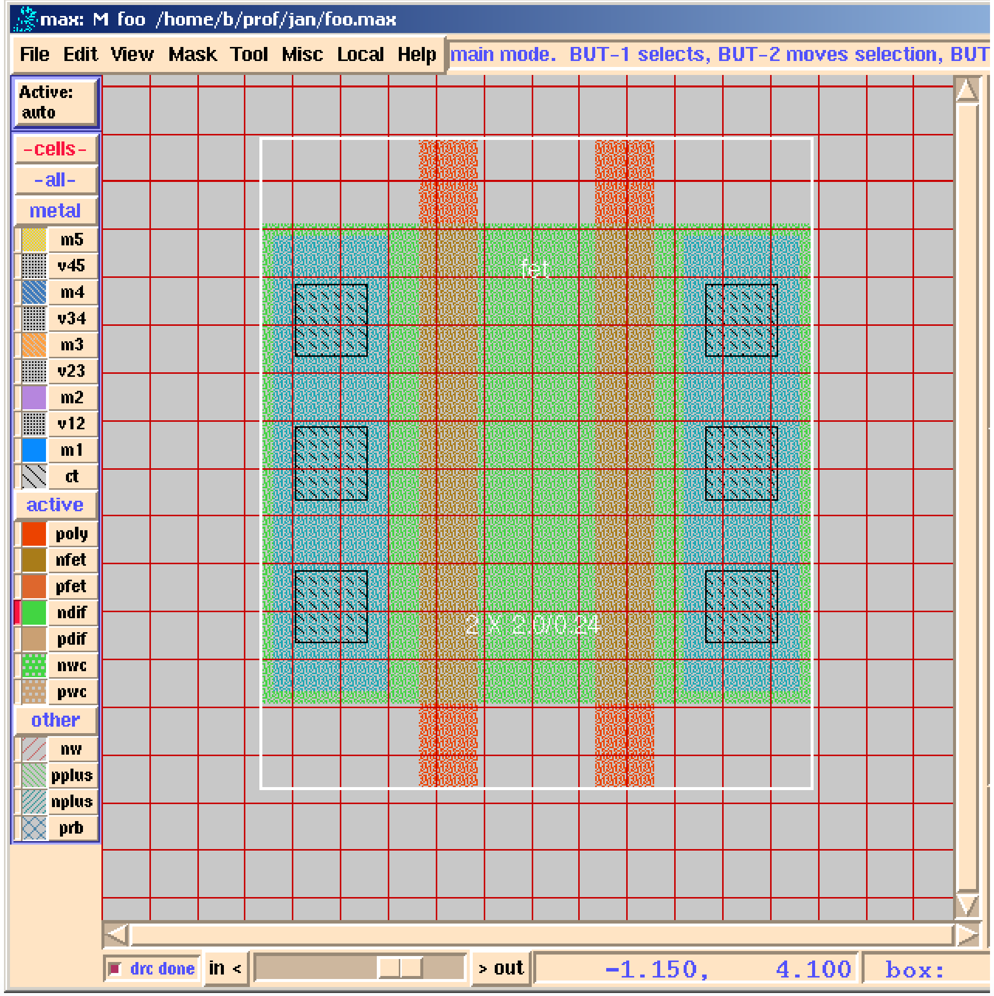


(a) Layout



(b) Cross-Section along A-A'

Layout Editor



max: M foo /home/b/prof/jan/foo.max

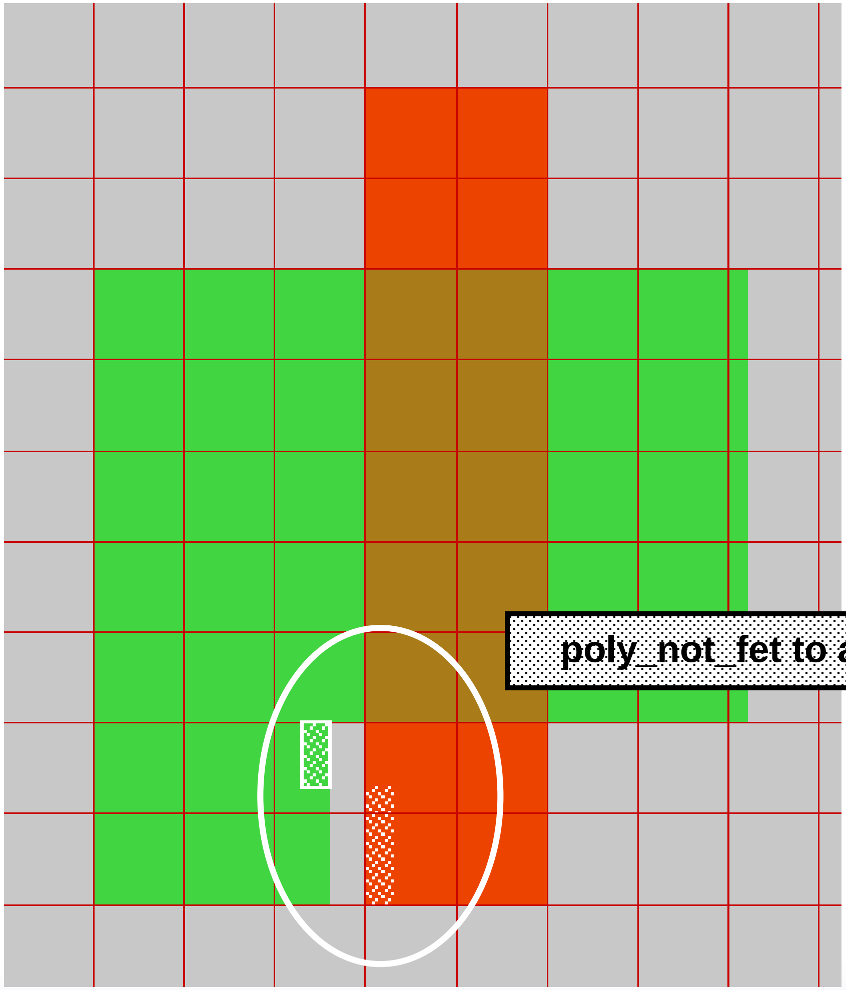
main mode. BUT-1 selects, BUT-2 moves selection, BUT

drc done

-1.150, 4.100

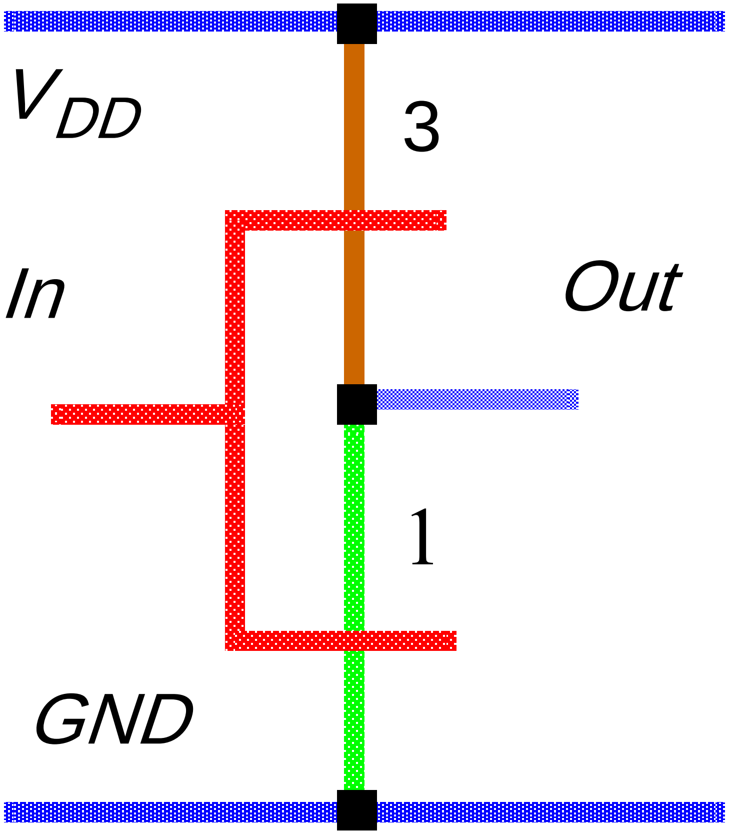
box:

Design Rule Checker



poly_not_fet to all_diff minimum spacing = 0.14 um.

Sticks Diagram



Stick diagram of inverter

- Dimensionless layout entities
- Only topology is important
- Final layout generated by "compaction" program

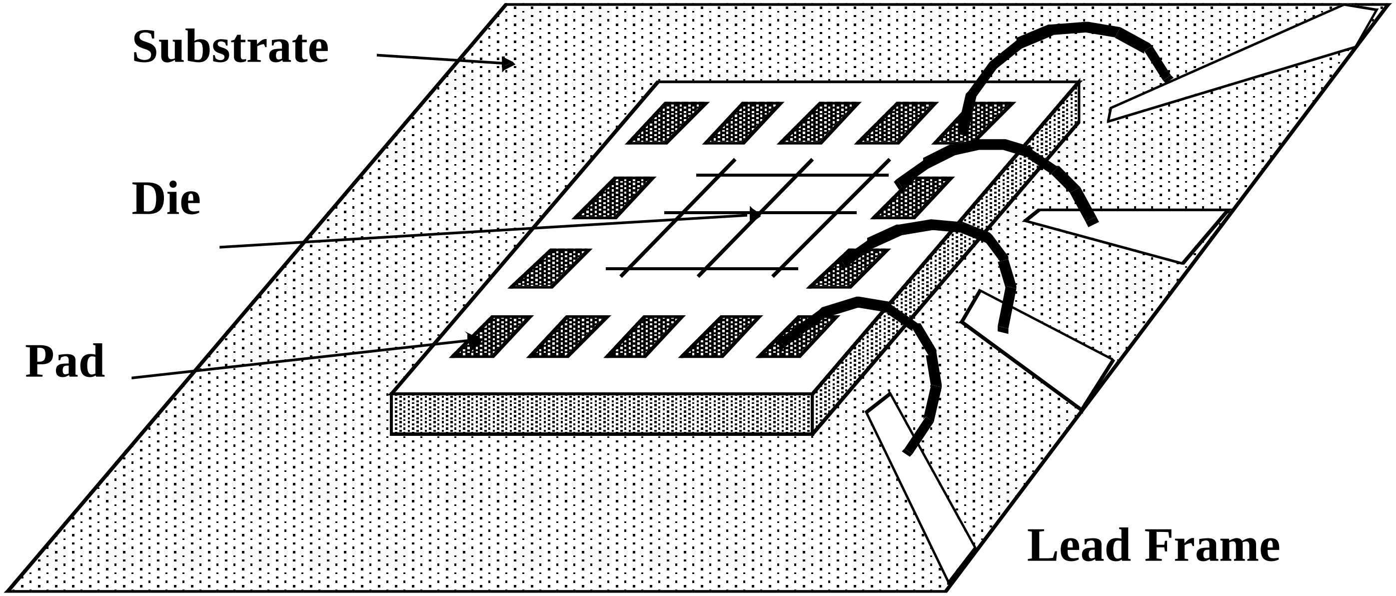
Packaging

Packaging Requirements

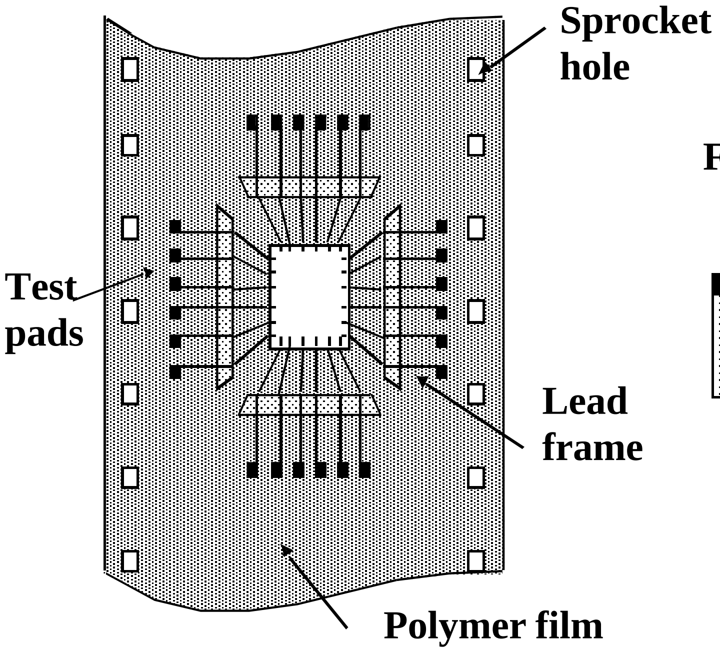
- Electrical: Low parasitics
- Mechanical: Reliable and robust
- Thermal: Efficient heat removal
- Economical: Cheap

Bonding Techniques

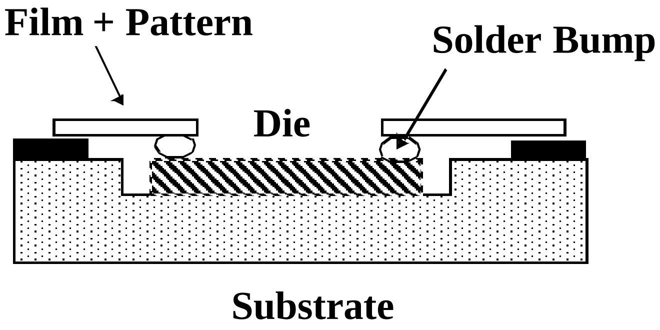
Wire Bonding



Tape-Automated Bonding (TAB)

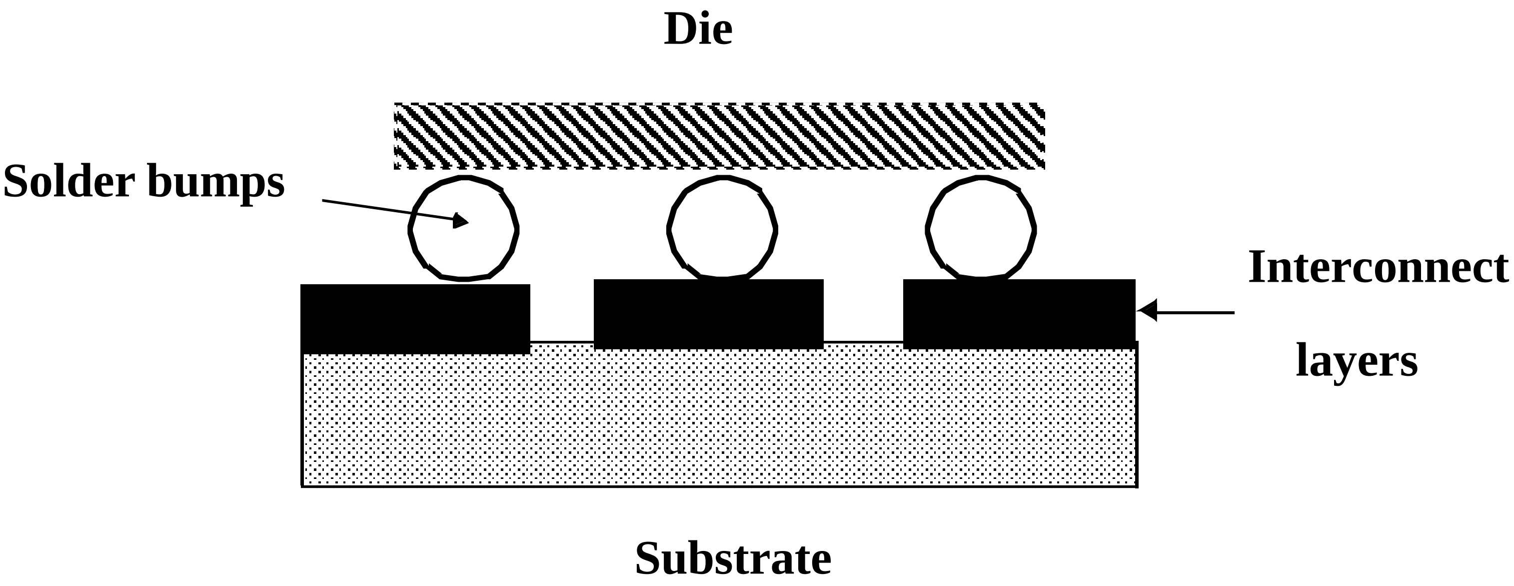


(a) Polymer Tape with imprinted wiring pattern.

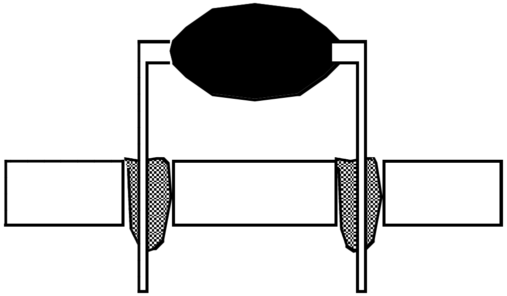


(b) Die attachment using solder bumps.

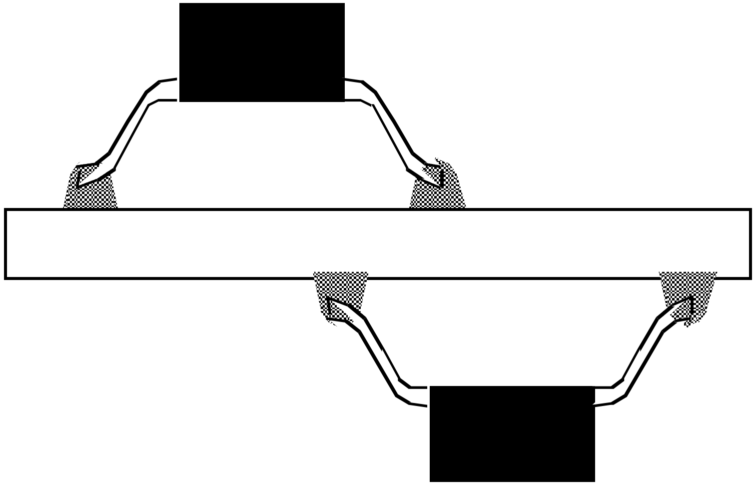
Flip-Chip Bonding



Package-to-Board Interconnect

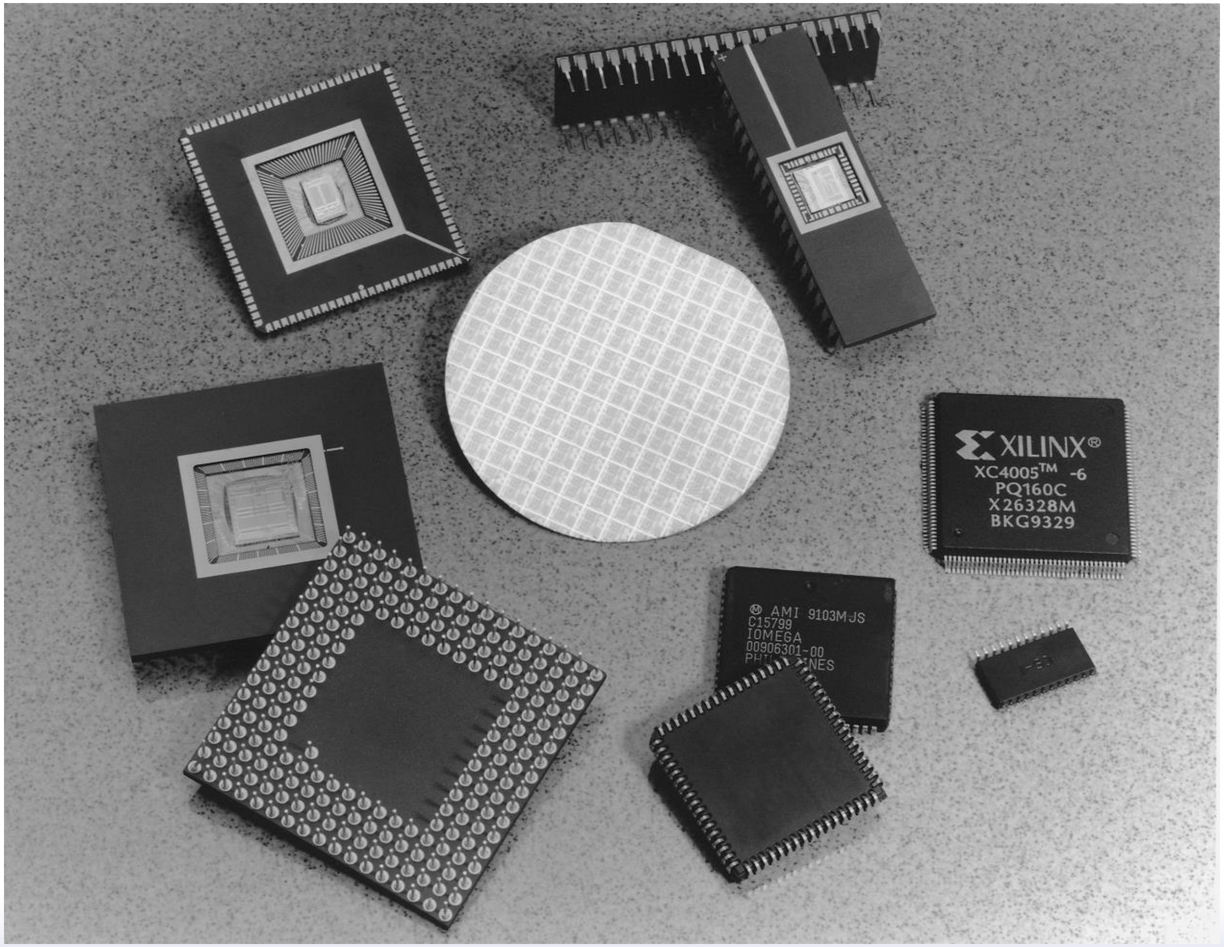


(a) Through-Hole Mounting

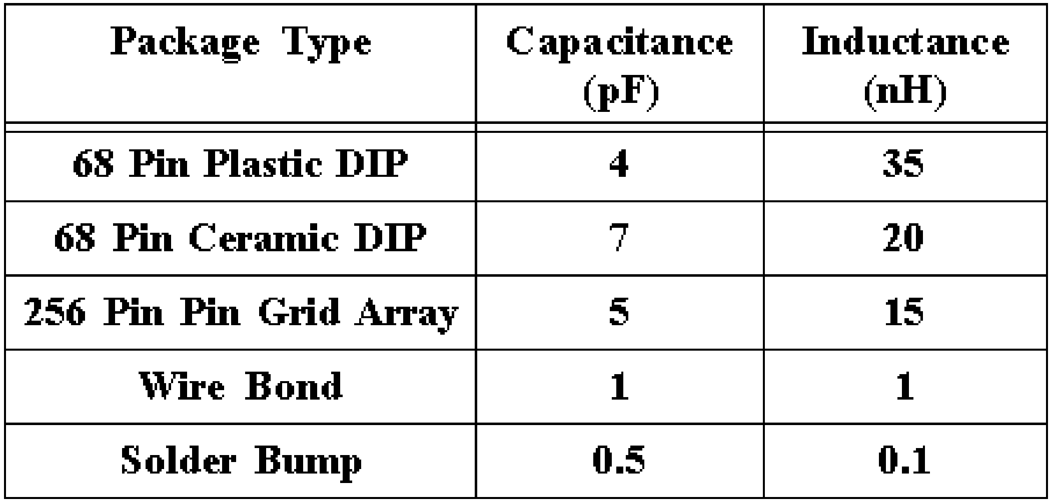


(b) Surface Mount

Package Types



Package Parameters



Package Type	Capacitance (pF)	Inductance (nH)
68 Pin Plastic DIP	4	35
68 Pin Ceramic DIP	7	20
256 Pin Pin Grid Array	5	15
Wire Bond	1	1
Solder Bump	0.5	0.1

Typical Capacitances and Inductances of Various Package and Bonding Styles (from [Sze83])

Multi-Chip Modules