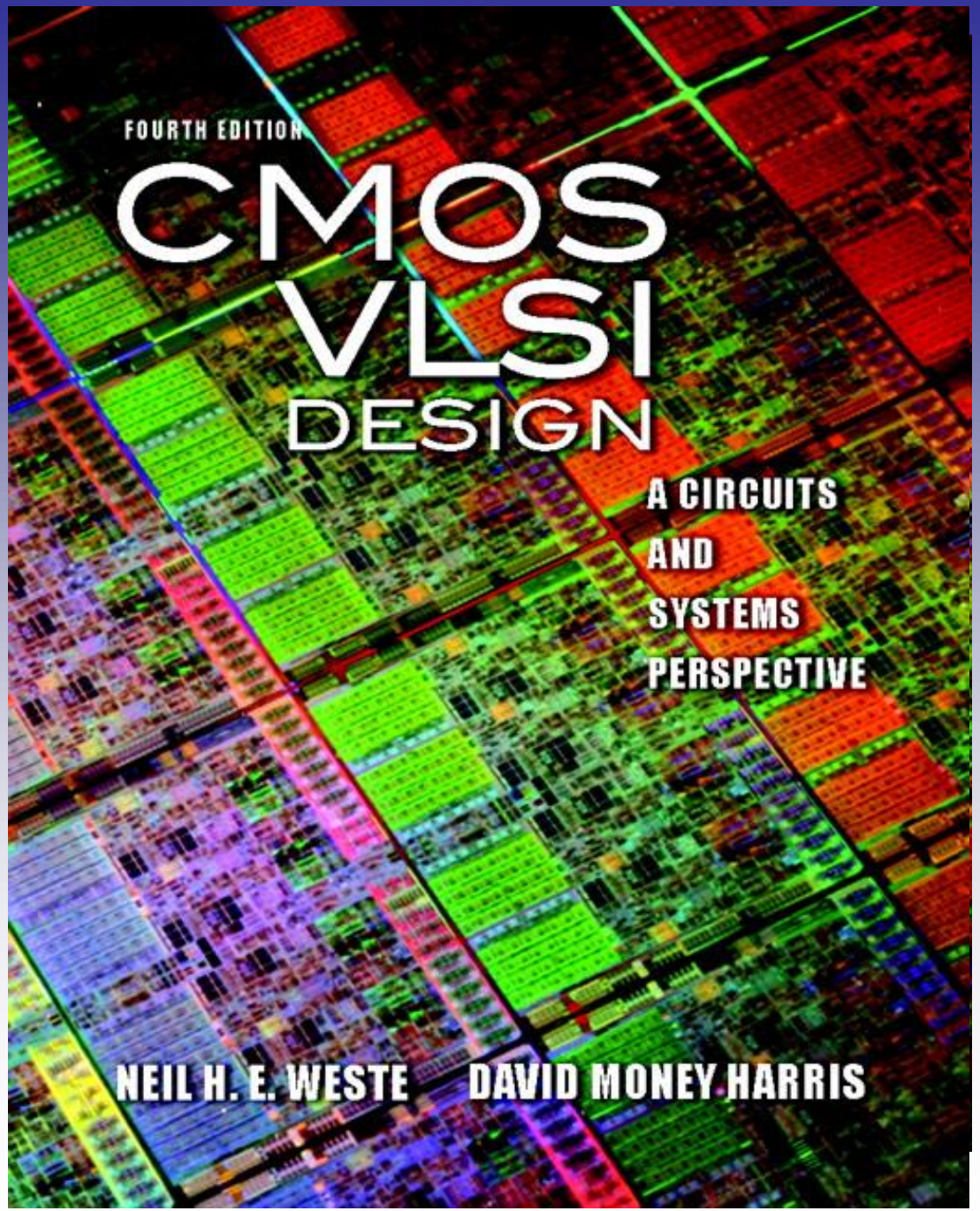
Chapter 1

Introduction



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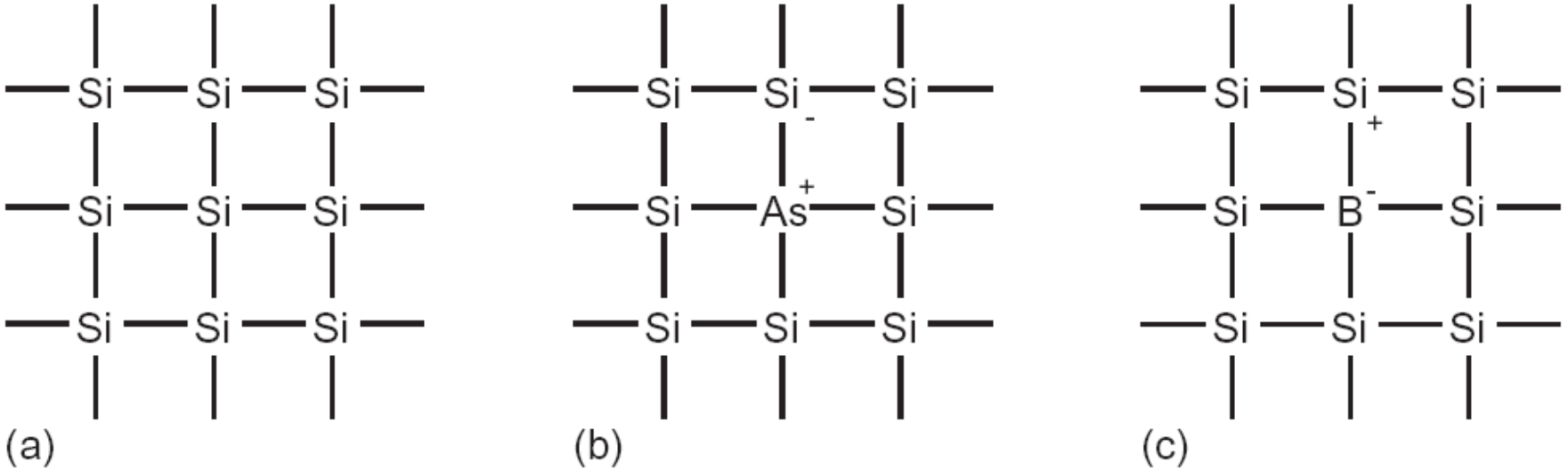

FIGURE 1.7 Silicon lattice and dopant atoms

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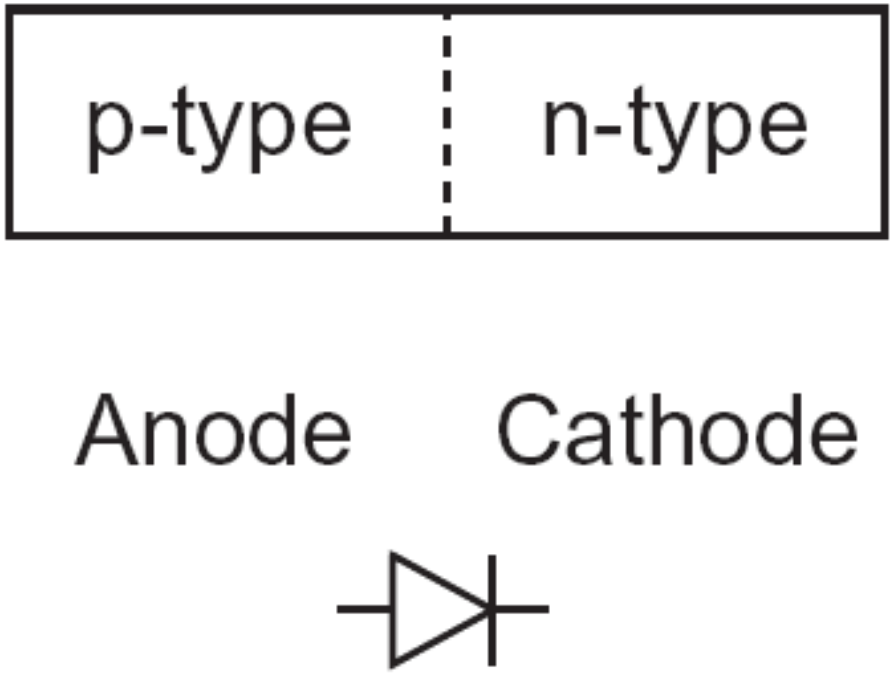

FIGURE 1.8
p-n junction diode structure and symbol

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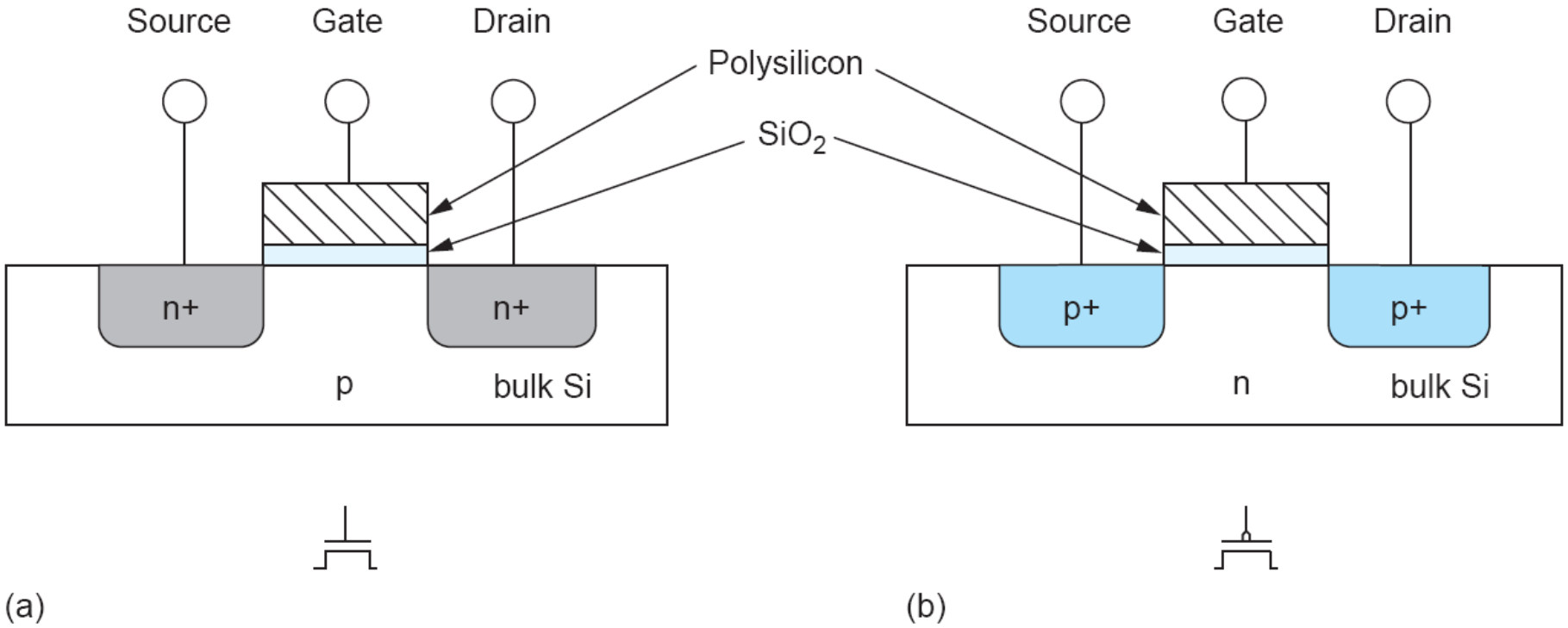

FIGURE 1.9 nMOS transistor (a) and pMOS transistor (b)

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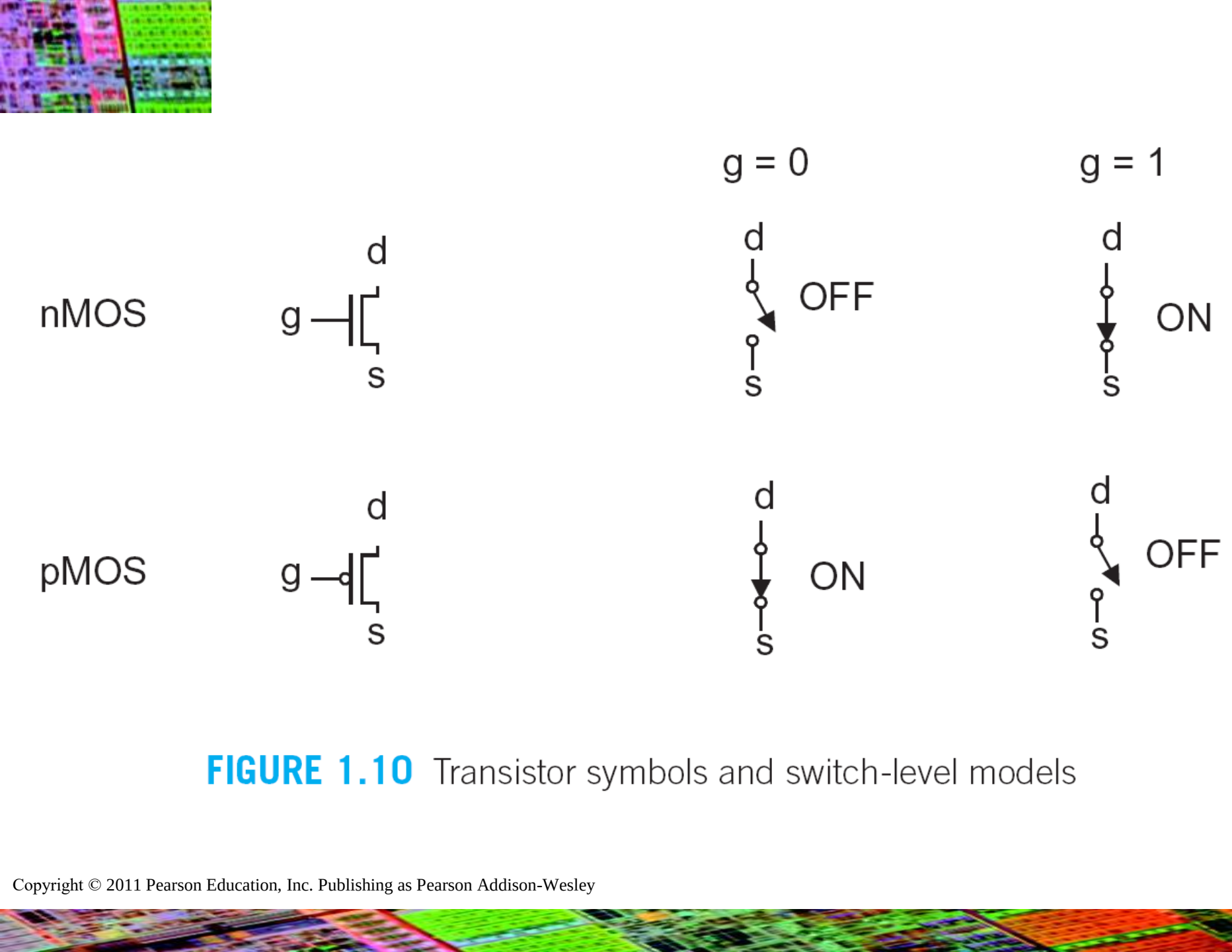

FIGURE 1.10 Transistor symbols and switch-level models

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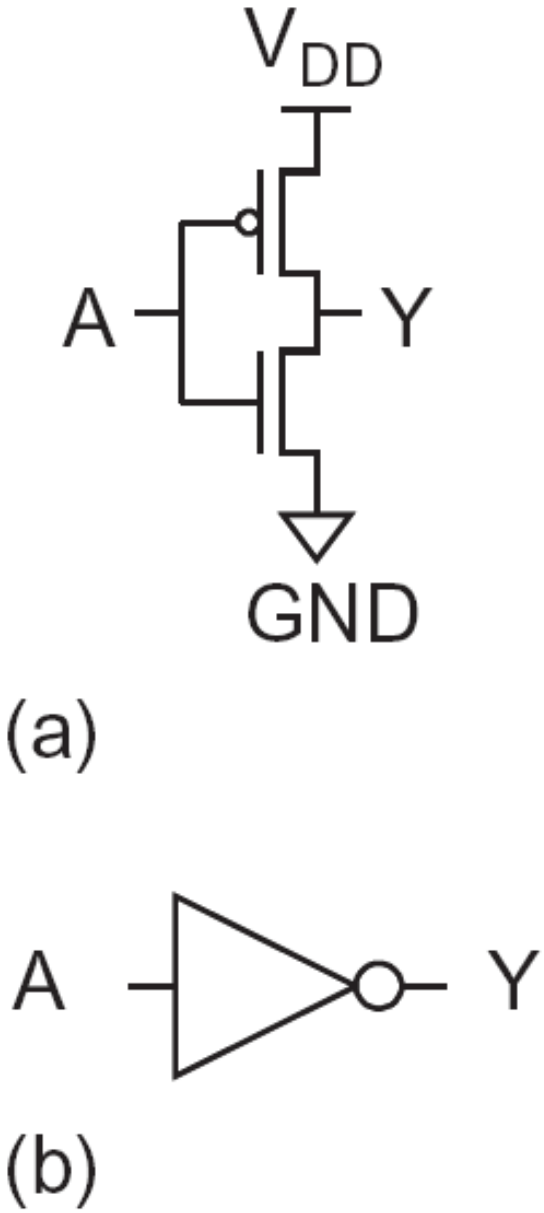

FIGURE 1.11
Inverter schematic
(a) and symbol
(b) $Y = \overline{A}$

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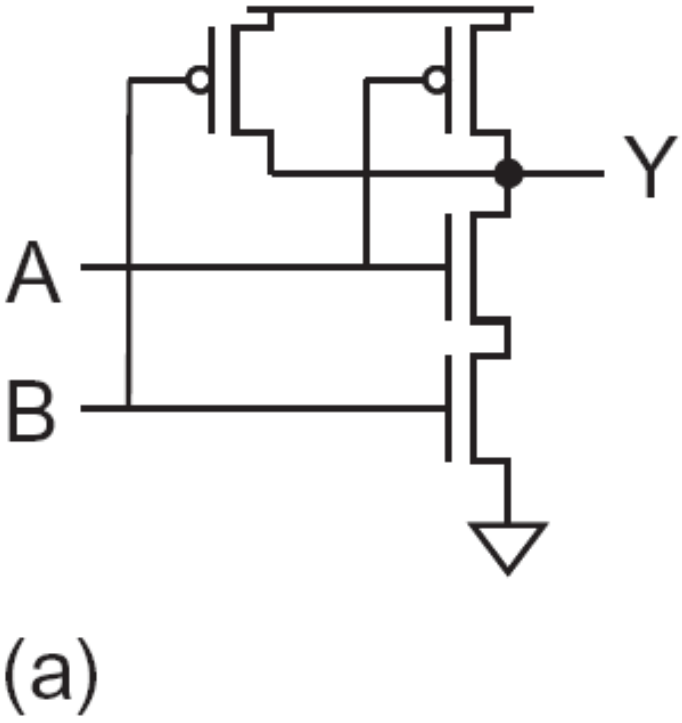

FIGURE 1.12 2-input NAND gate schematic (a) and symbol (b) $Y = \overline{A \cdot B}$

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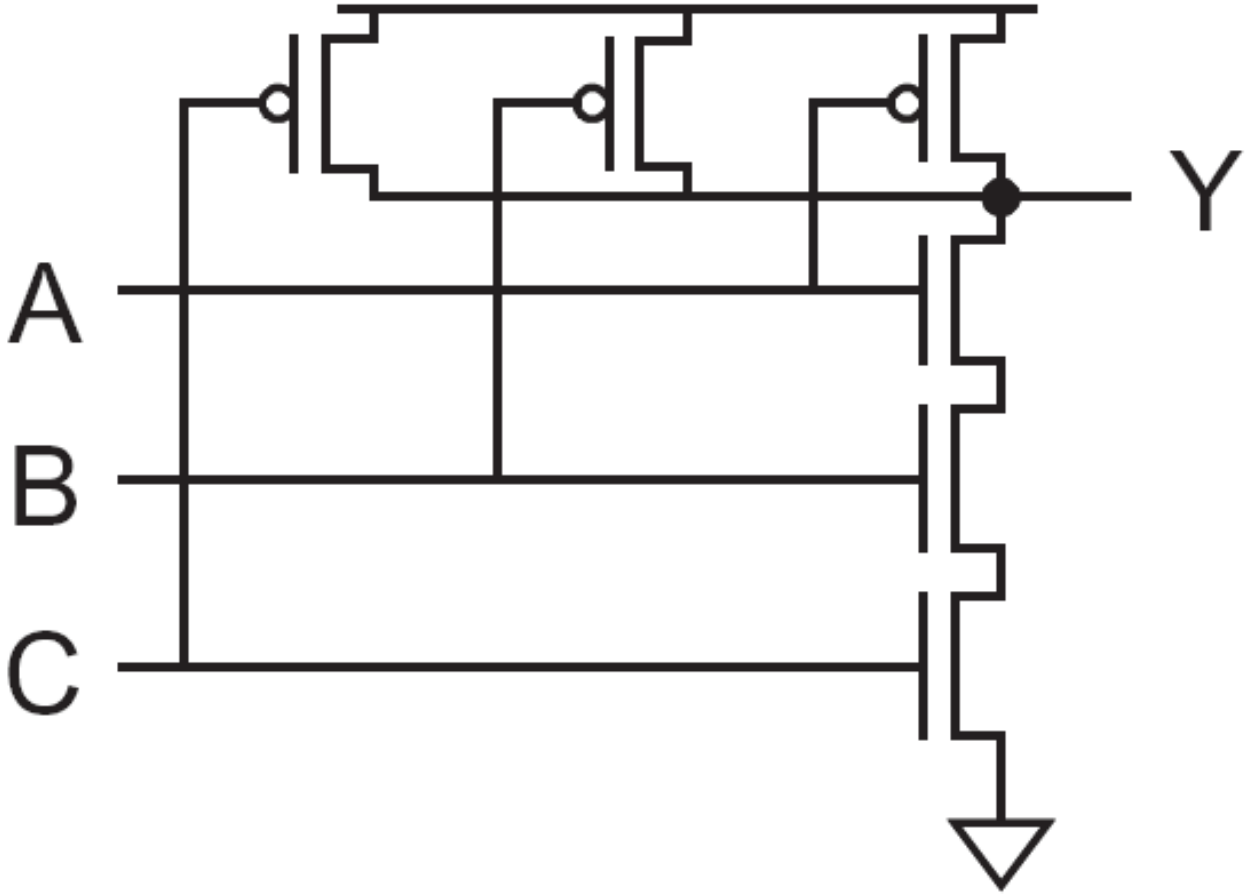

FIGURE 1.13 3-input NAND gate schematic $Y = \overline{A \cdot B \cdot C}$

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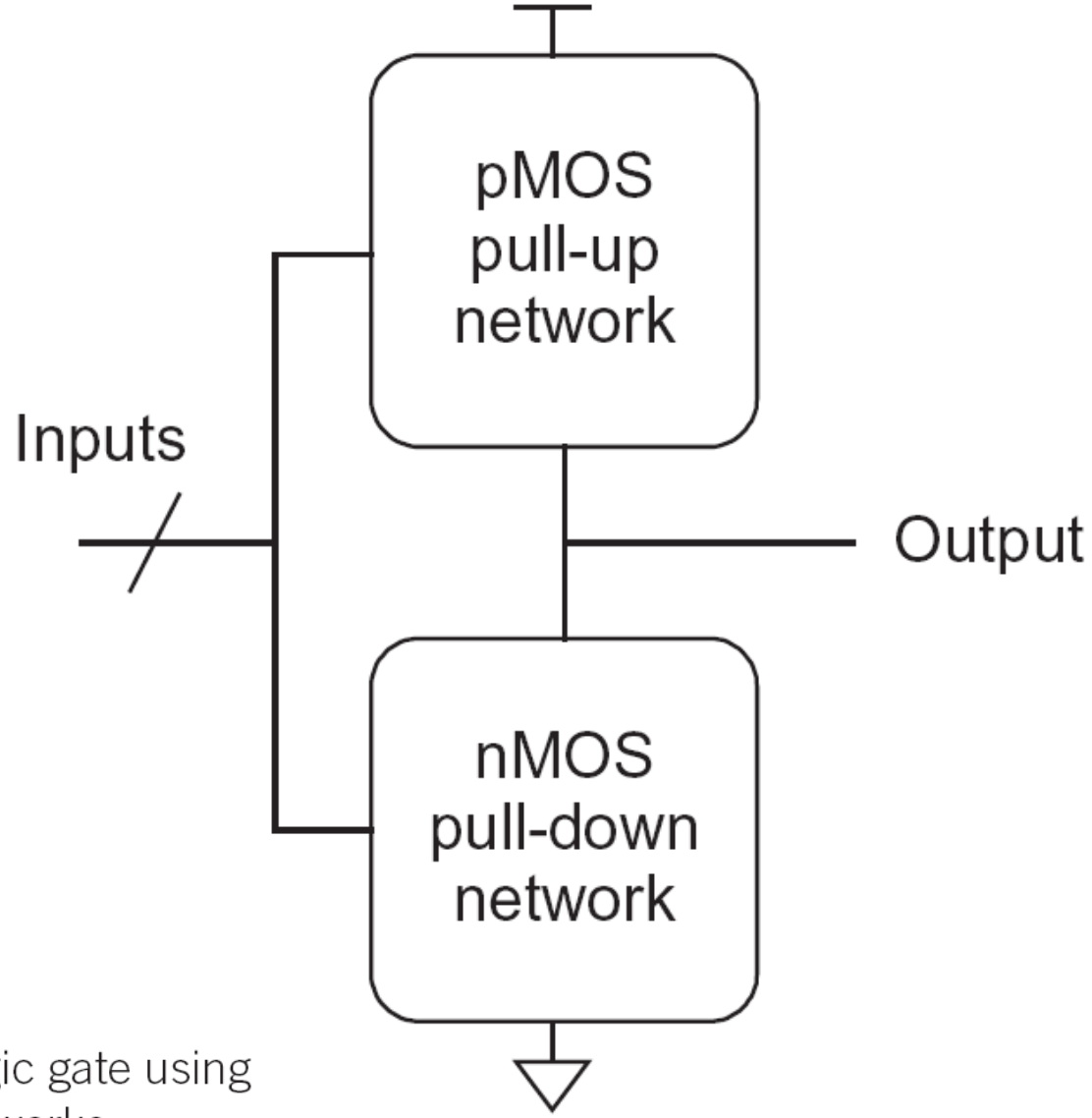

FIGURE 1.14 General logic gate using pull-up and pull-down networks

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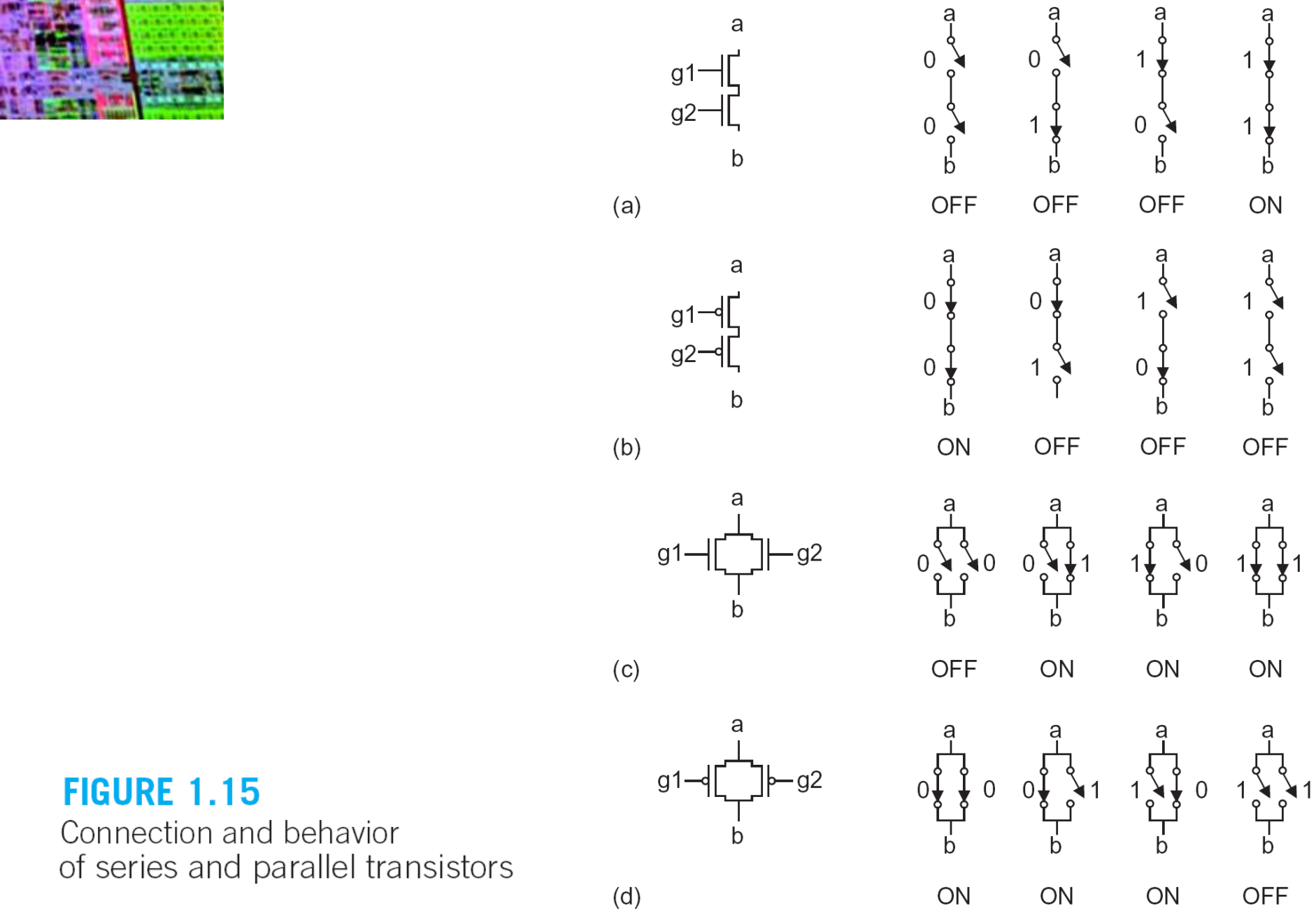

FIGURE 1.15
Connection and behavior of series and parallel transistors

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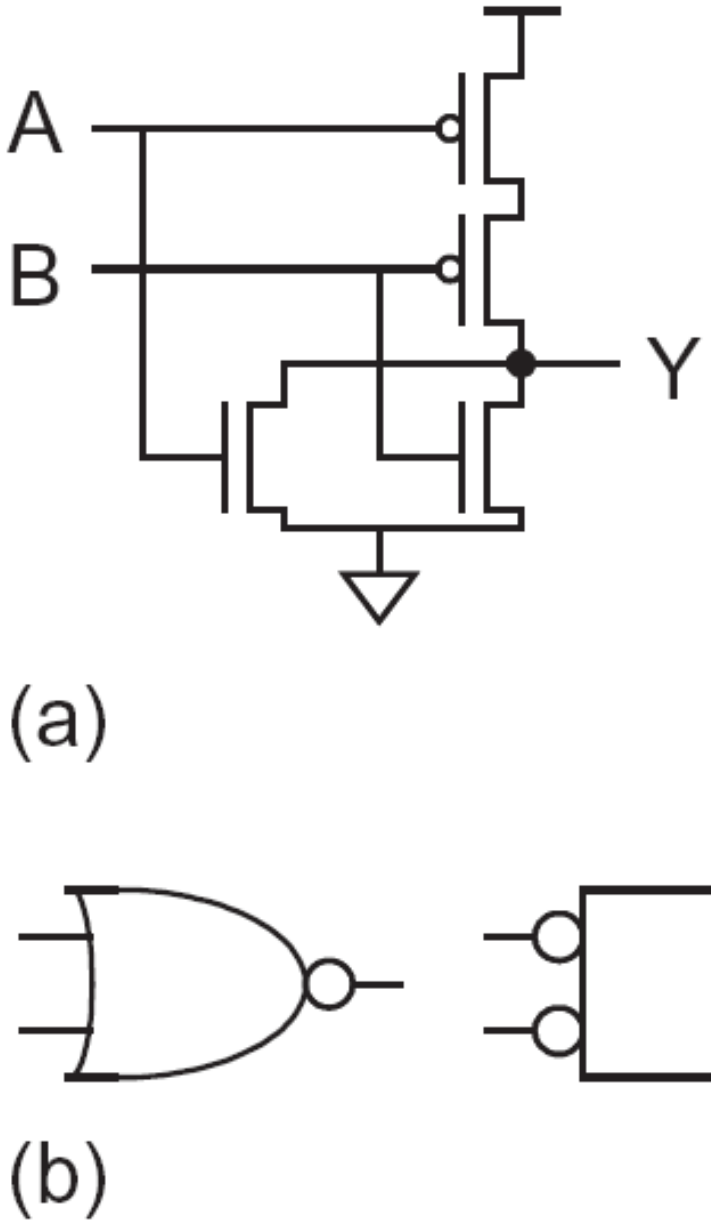

FIGURE 1.16 2-input NOR gate schematic (a) and symbol (b) $Y = \overline{A + B}$

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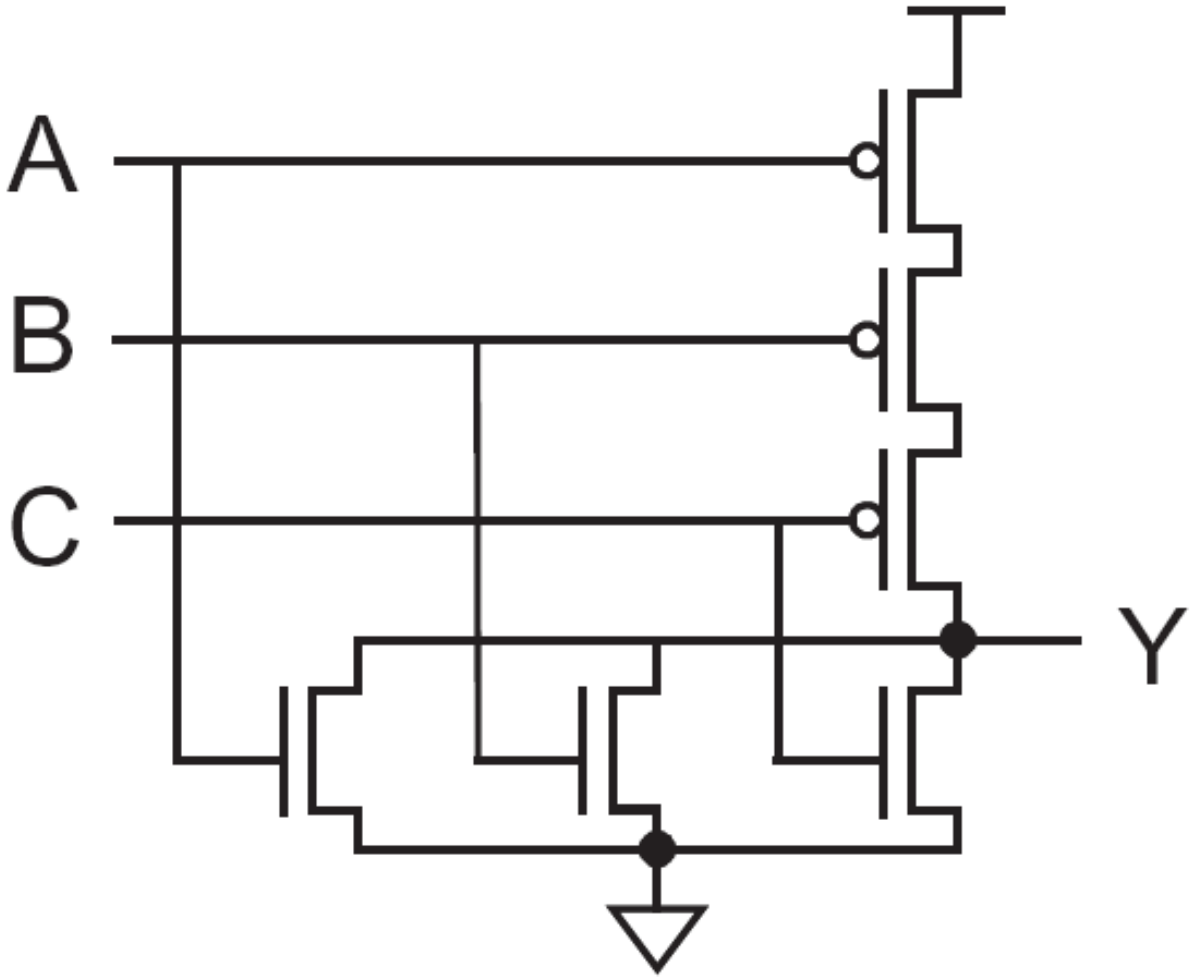

FIGURE 1.17 3-input NOR gate schematic $Y = \overline{A + B + C}$

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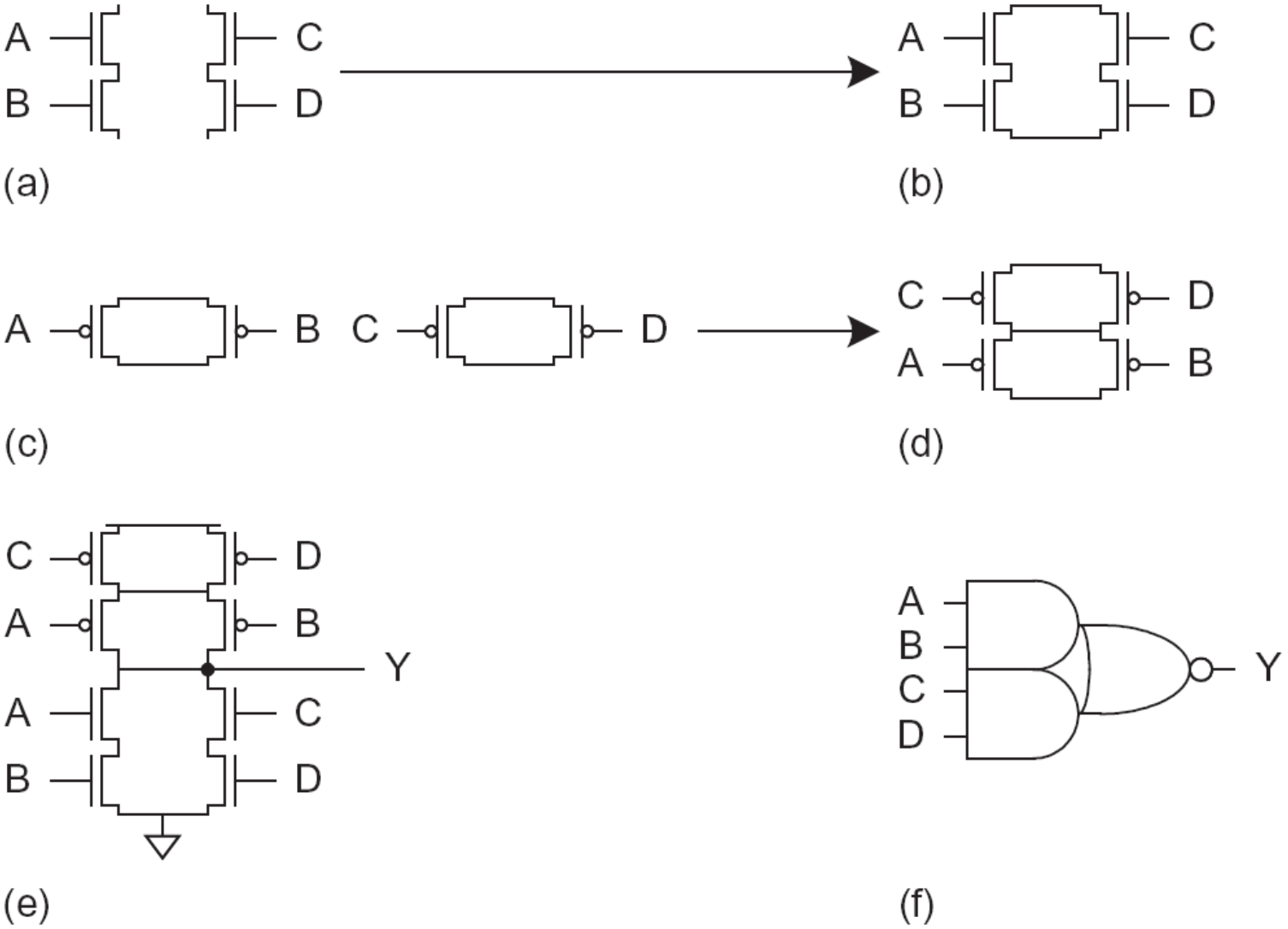

FIGURE 1.18 CMOS compound gate for function $Y = \overline{(A \cdot B) + (C \cdot D)}$

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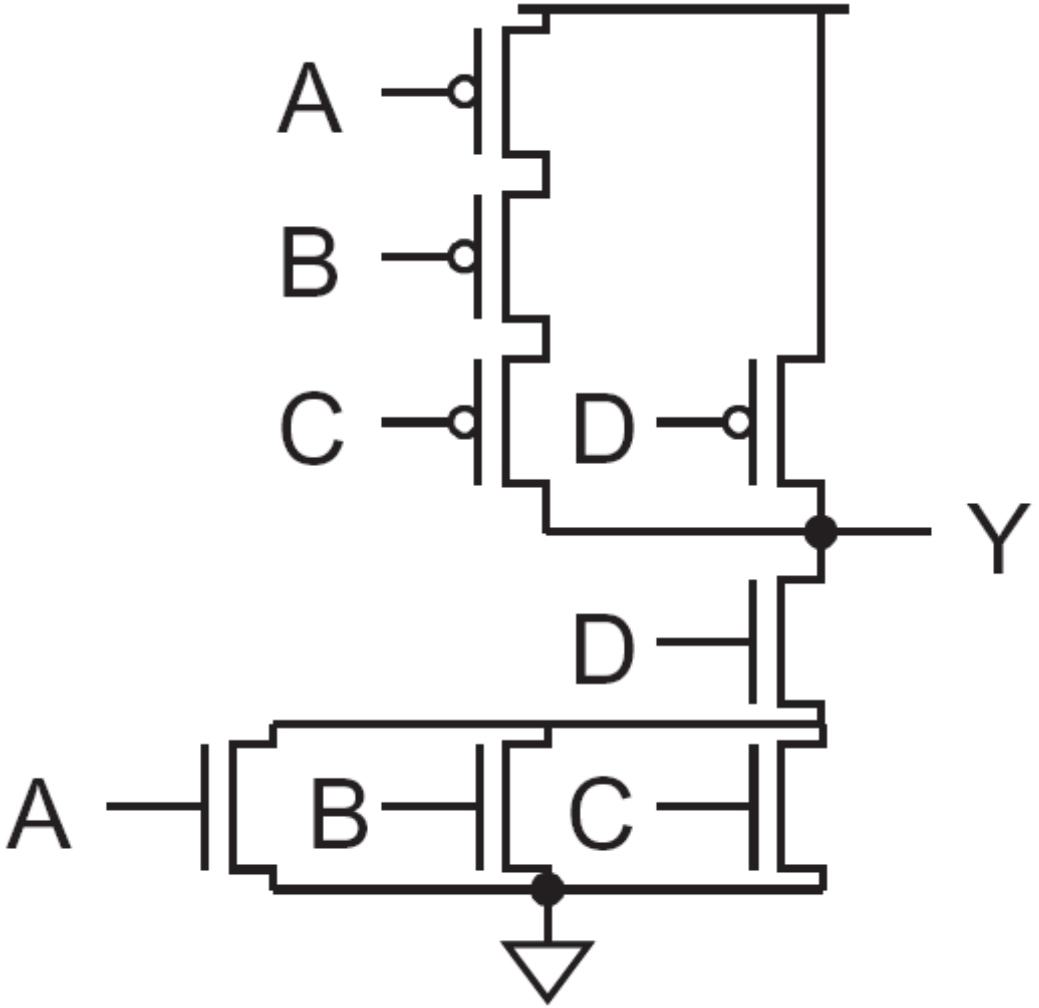

FIGURE 1.19
CMOS compound gate for function
$Y = \overline{(A + B + C) \cdot D}$

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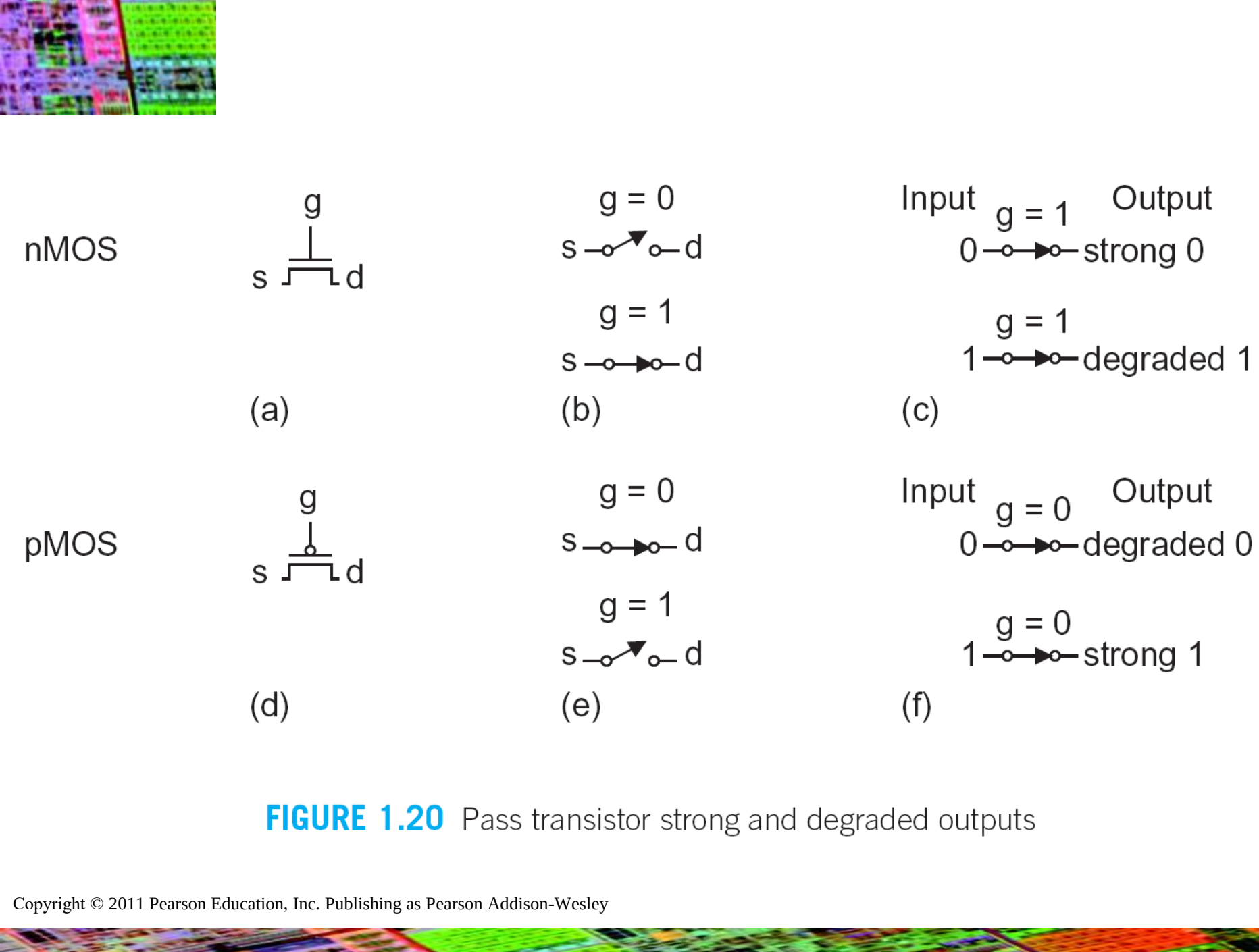

FIGURE 1.20 Pass transistor strong and degraded outputs

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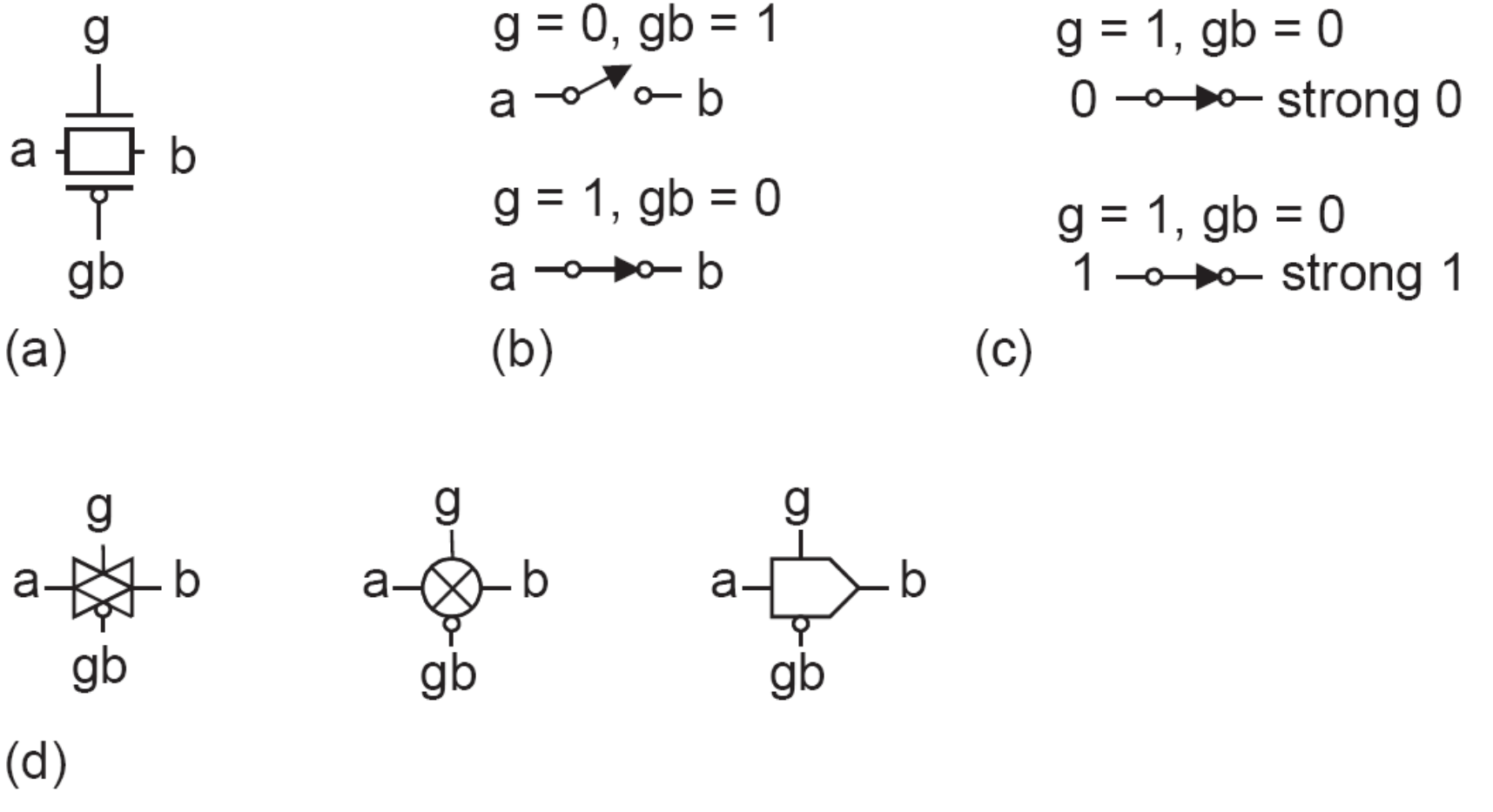

FIGURE 1.21 Transmission gate

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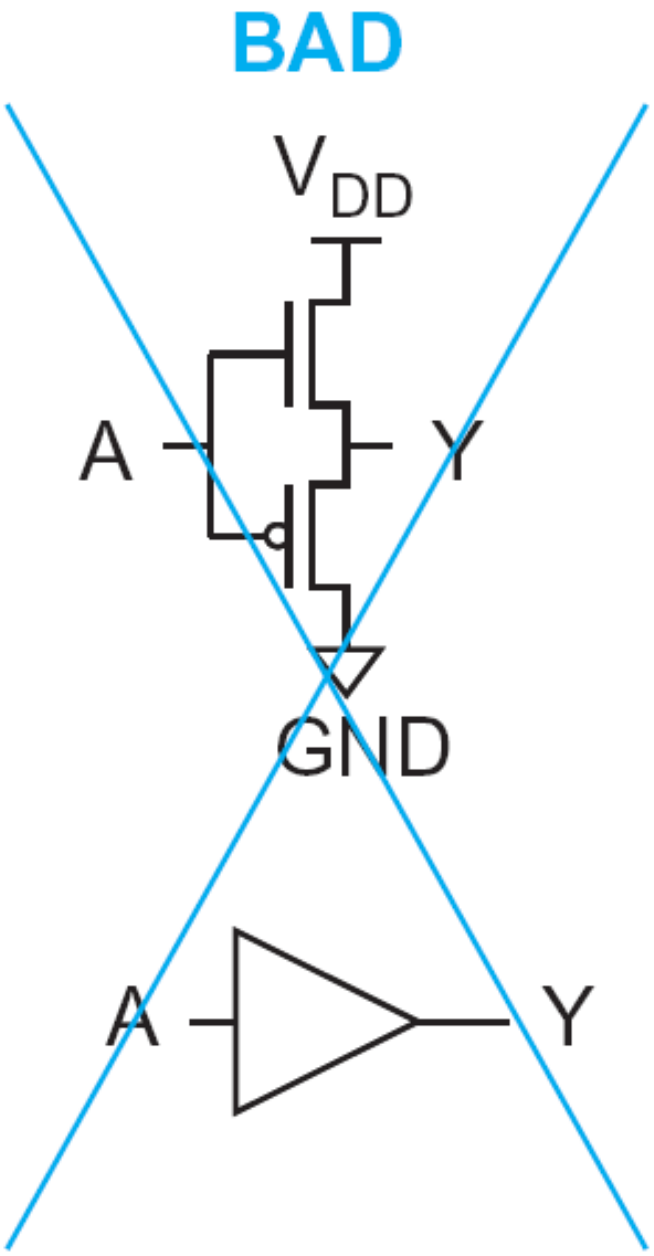

FIGURE 1.22
Bad noninverting buffer

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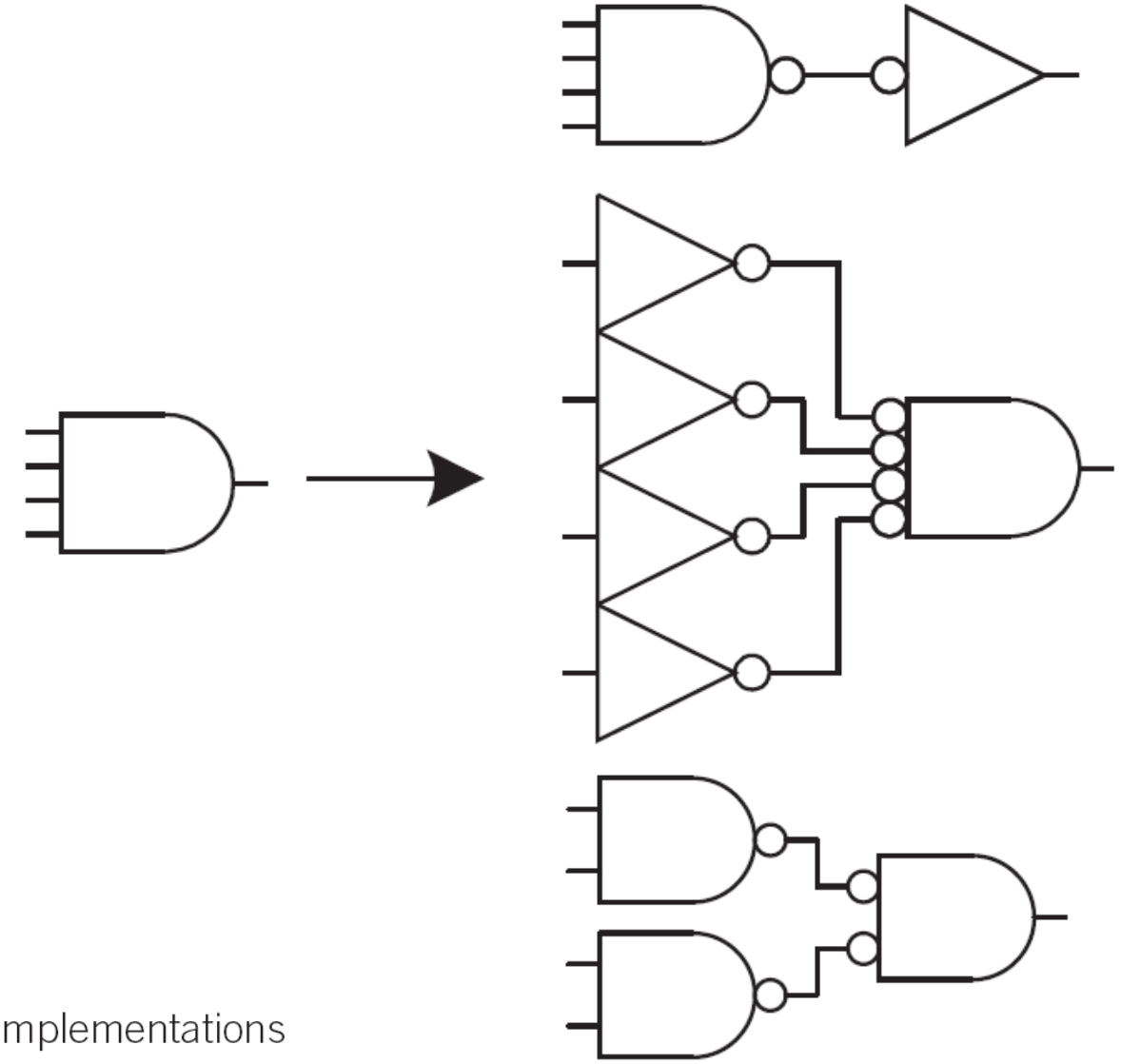

FIGURE 1.23 Various implementations of a CMOS 4-input AND gate

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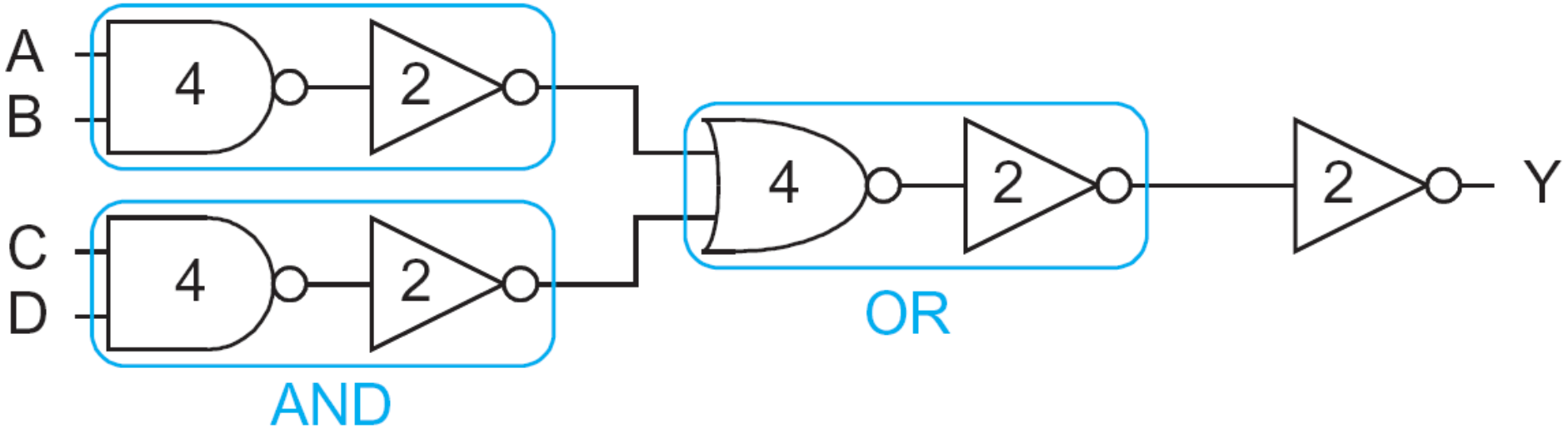

FIGURE 1.24 Inefficient discrete gate implementation of AOI22 with transistor counts indicated

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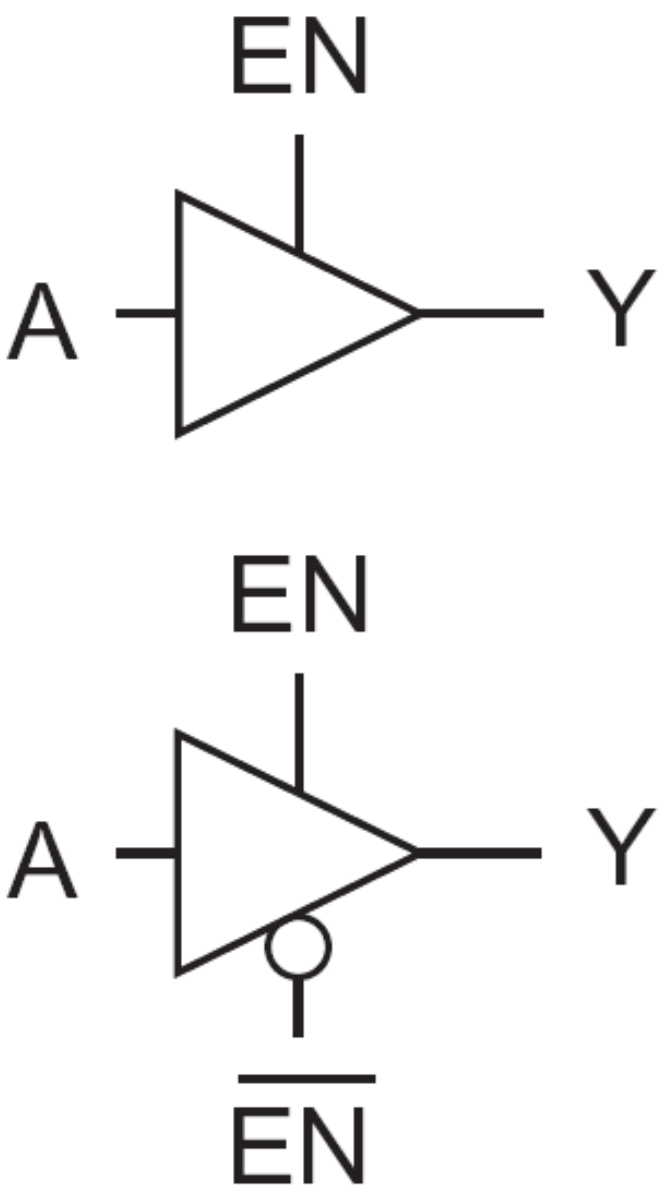

FIGURE 1.25
Tristate buffer symbol

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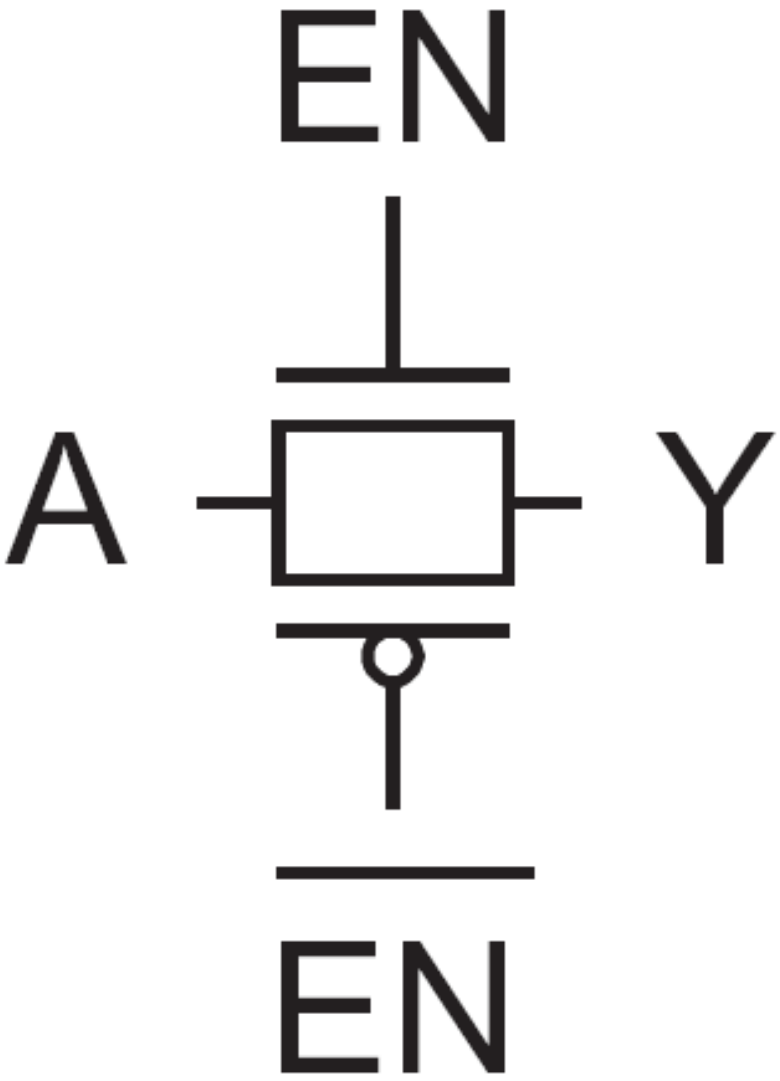

FIGURE 1.26
Transmission gate

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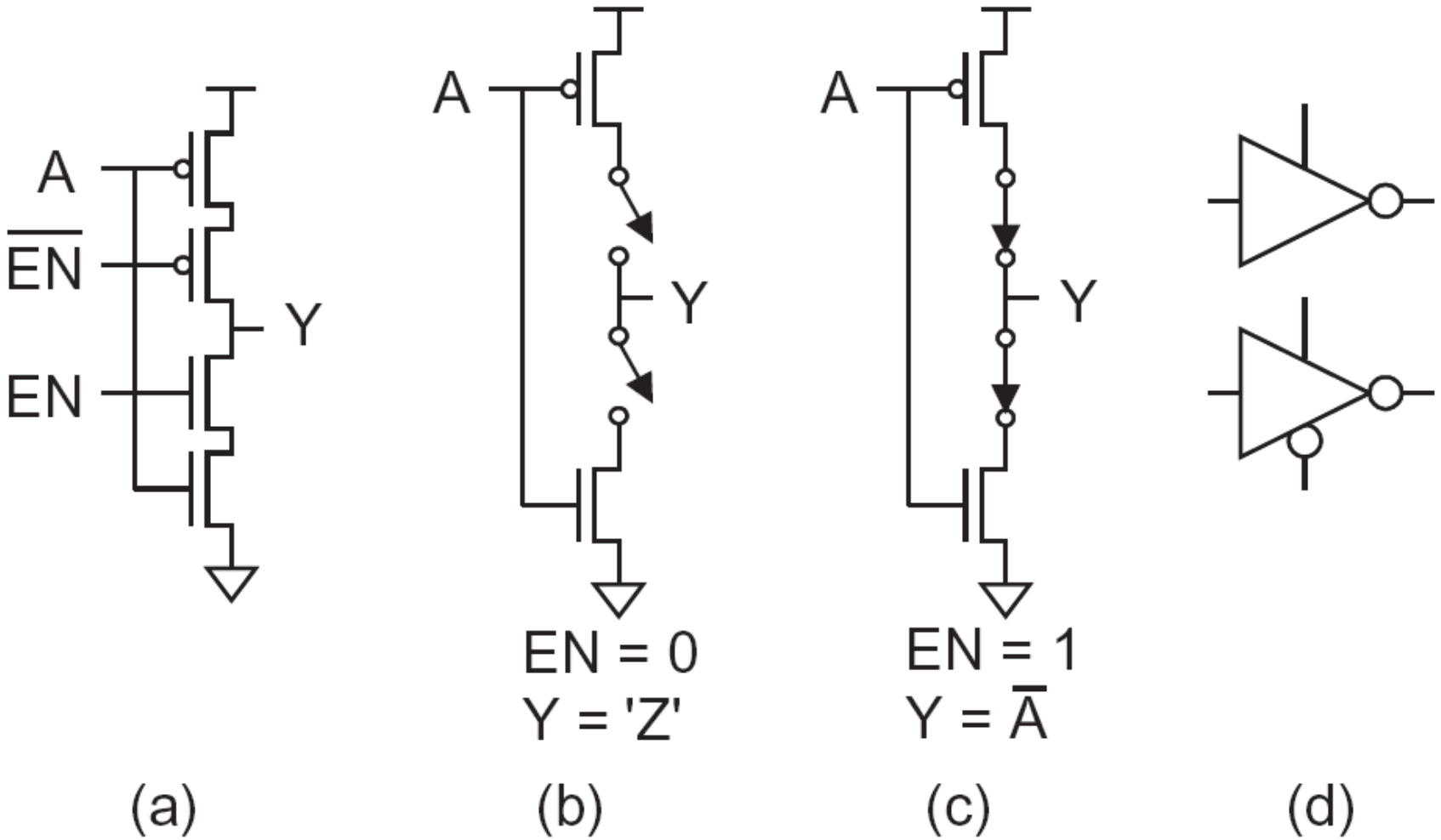

FIGURE 1.27 Tristate Inverter

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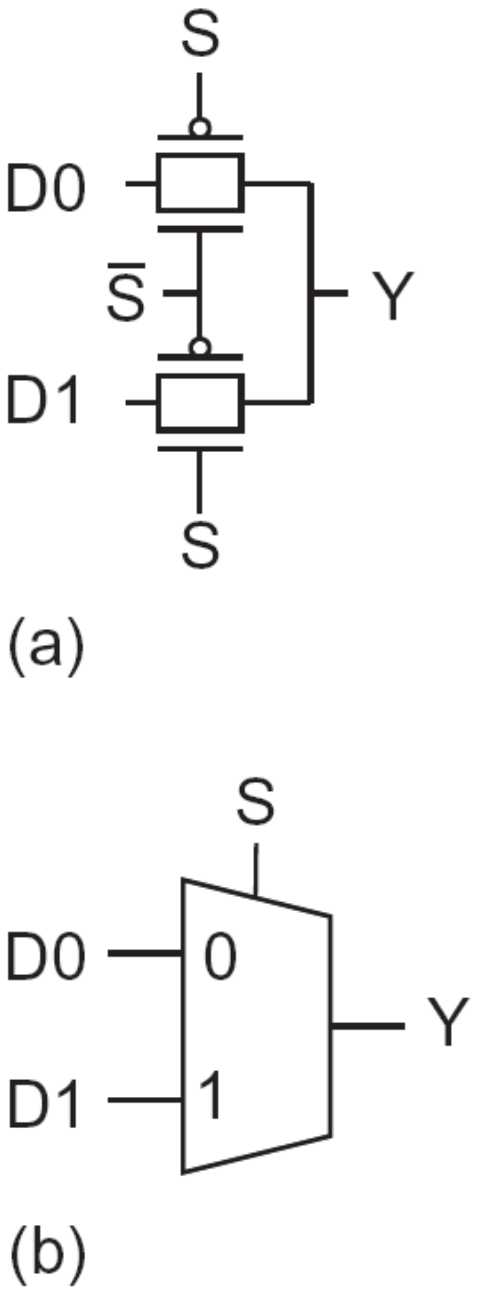

FIGURE 1.28 Transmission gate multiplexer

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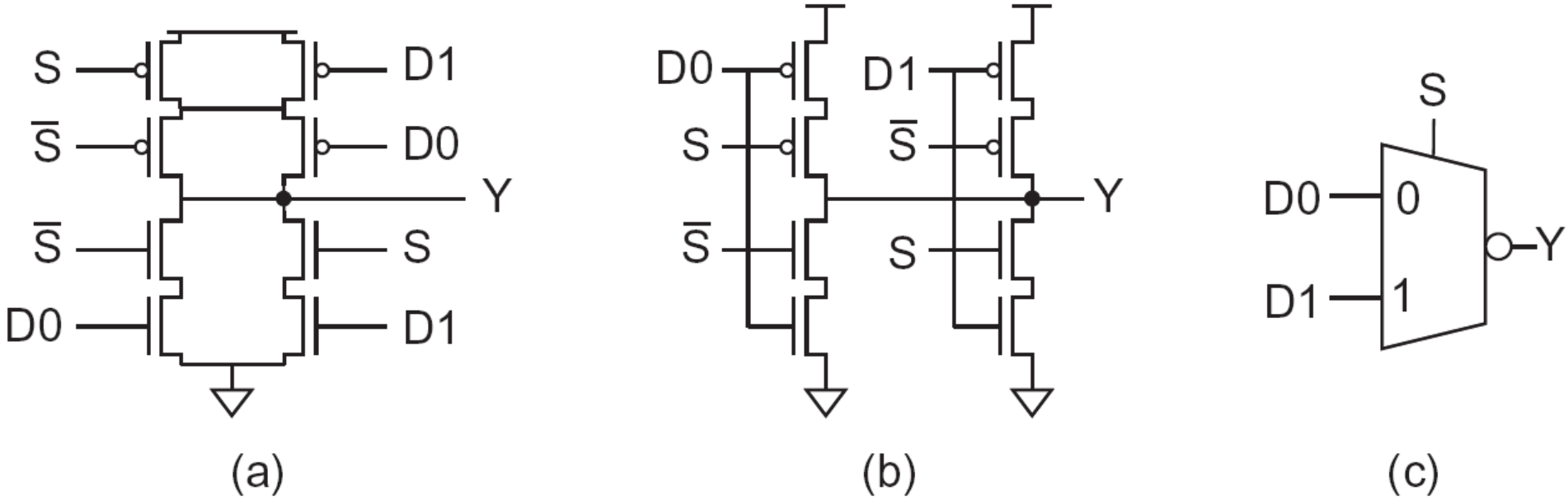

FIGURE 1.29 Inverting multiplexer

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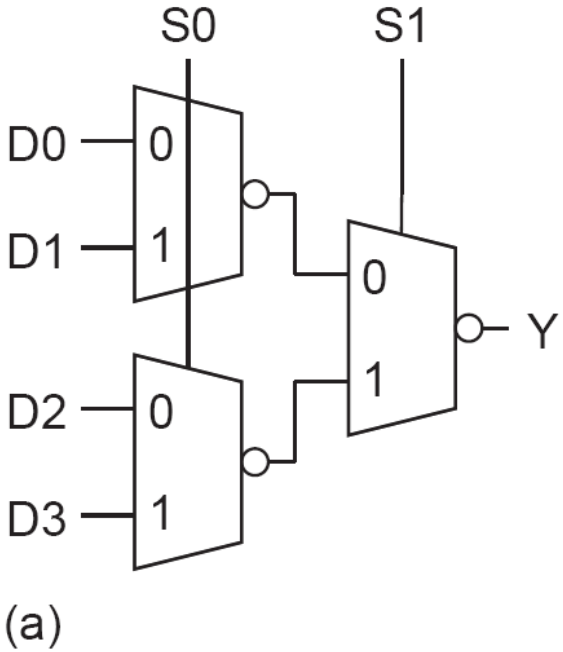
FIGURE 1.30 4:1 multiplexer



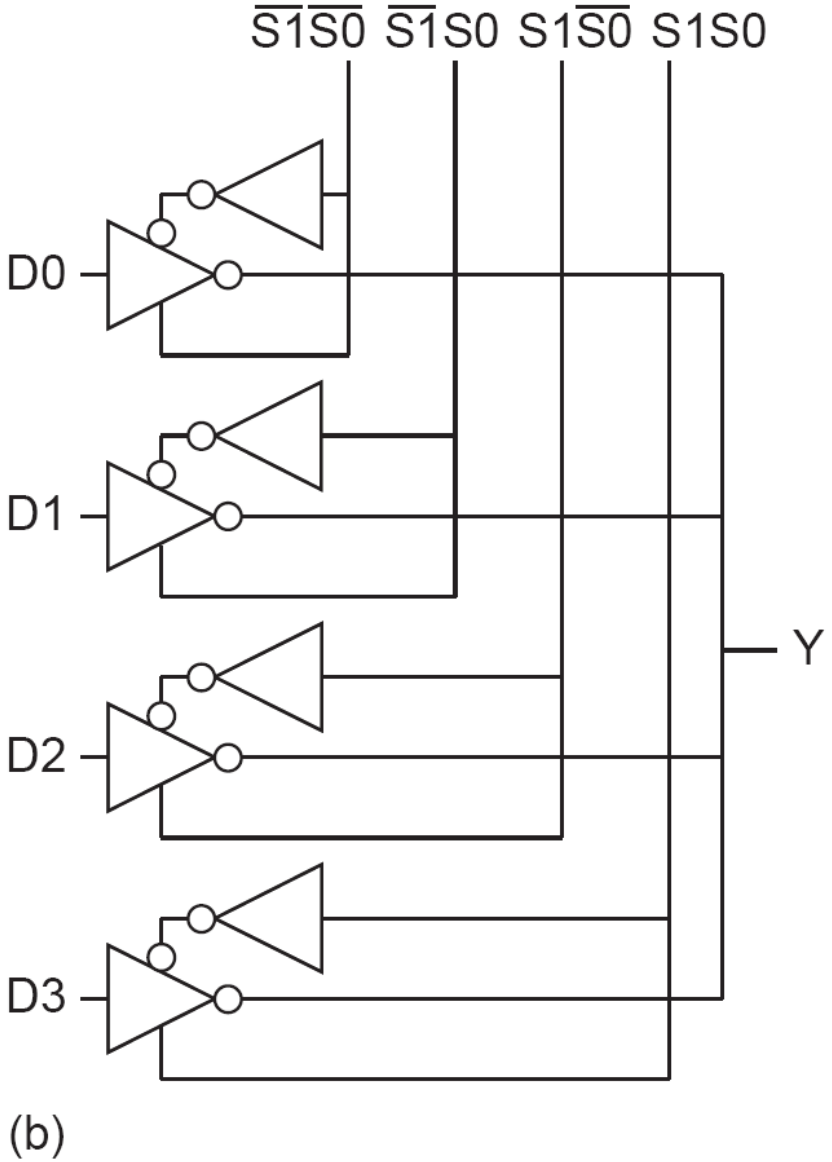


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FIGURE 1.31 CMOS positive-level-sensitive *D* latch

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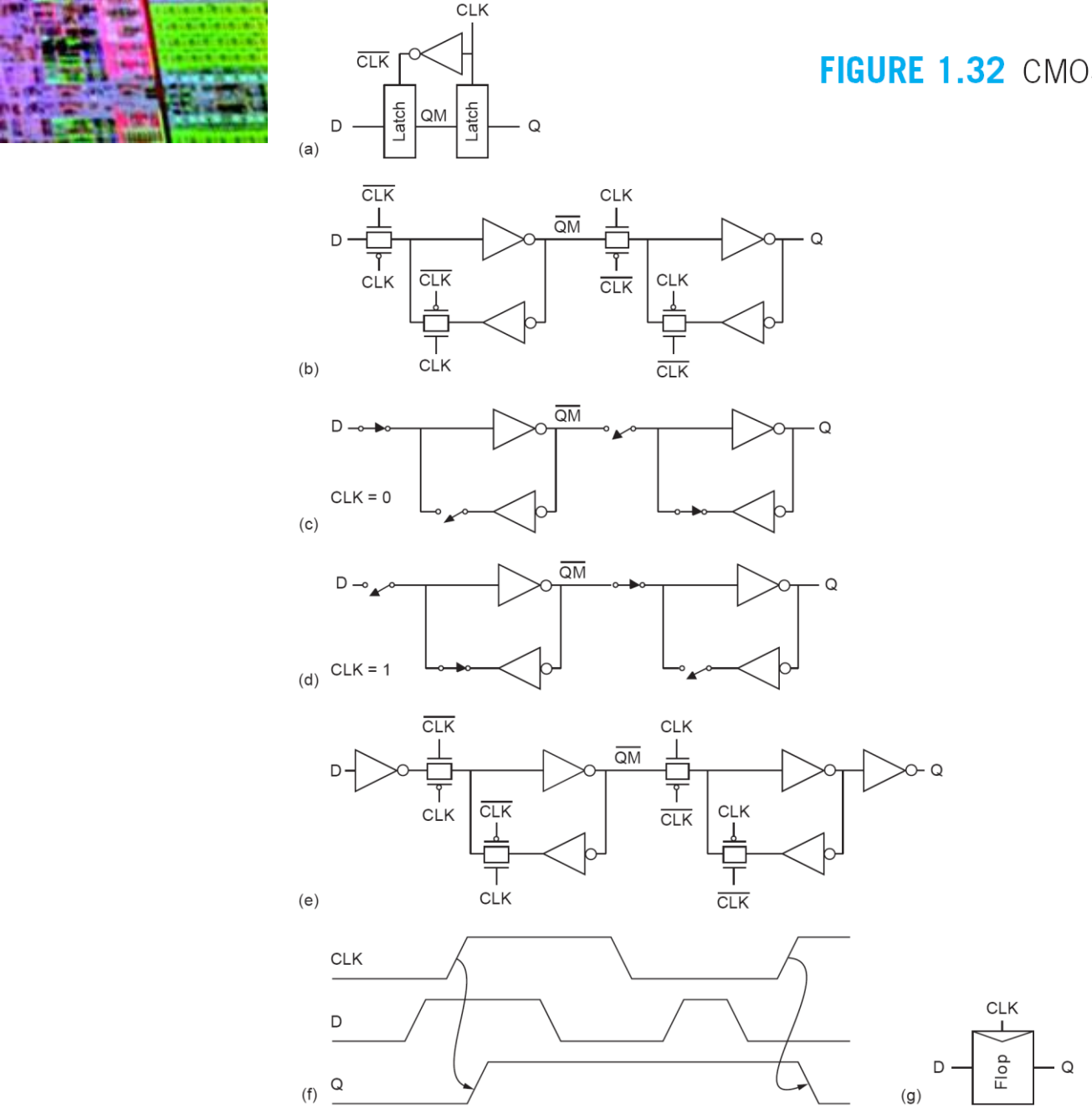

FIGURE 1.32 CMOS positive-edge-triggered *D* flip-flop

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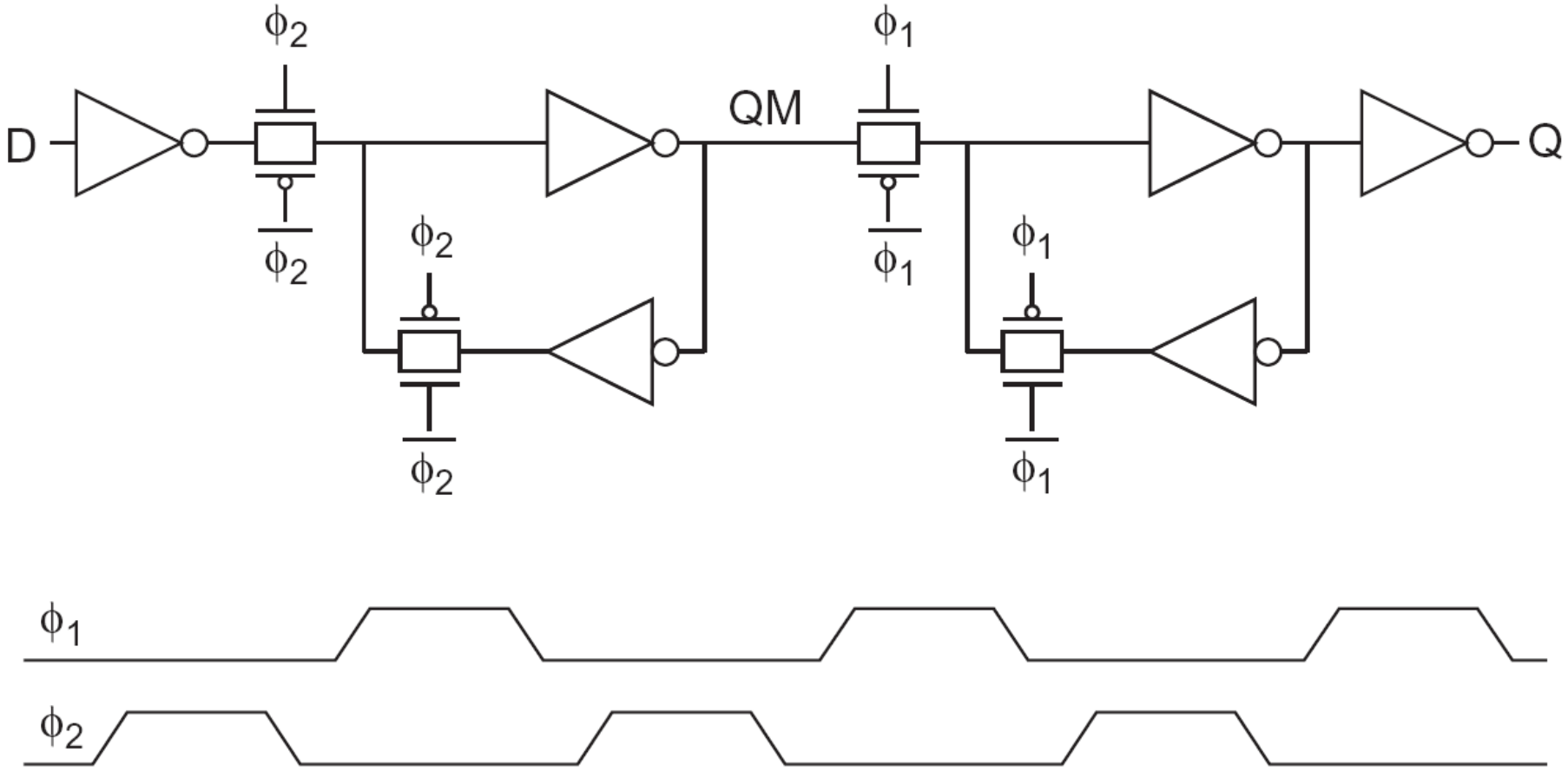

FIGURE 1.33 CMOS flip-flop with two-phase nonoverlapping clocks

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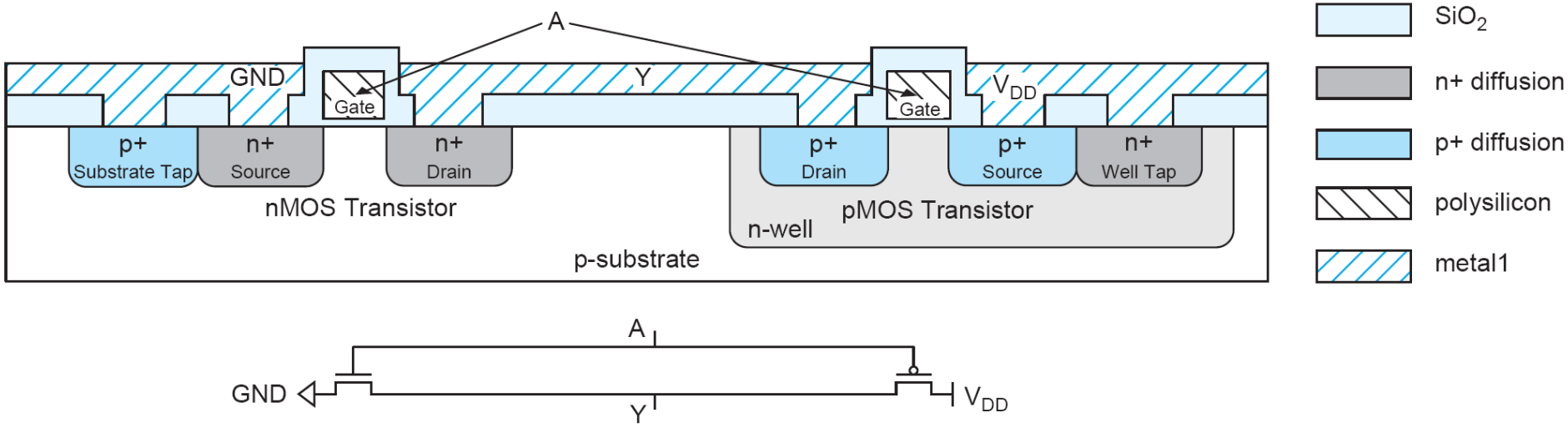

FIGURE 1.34 Inverter cross-section with well and substrate contacts. Color version on inside front cover.

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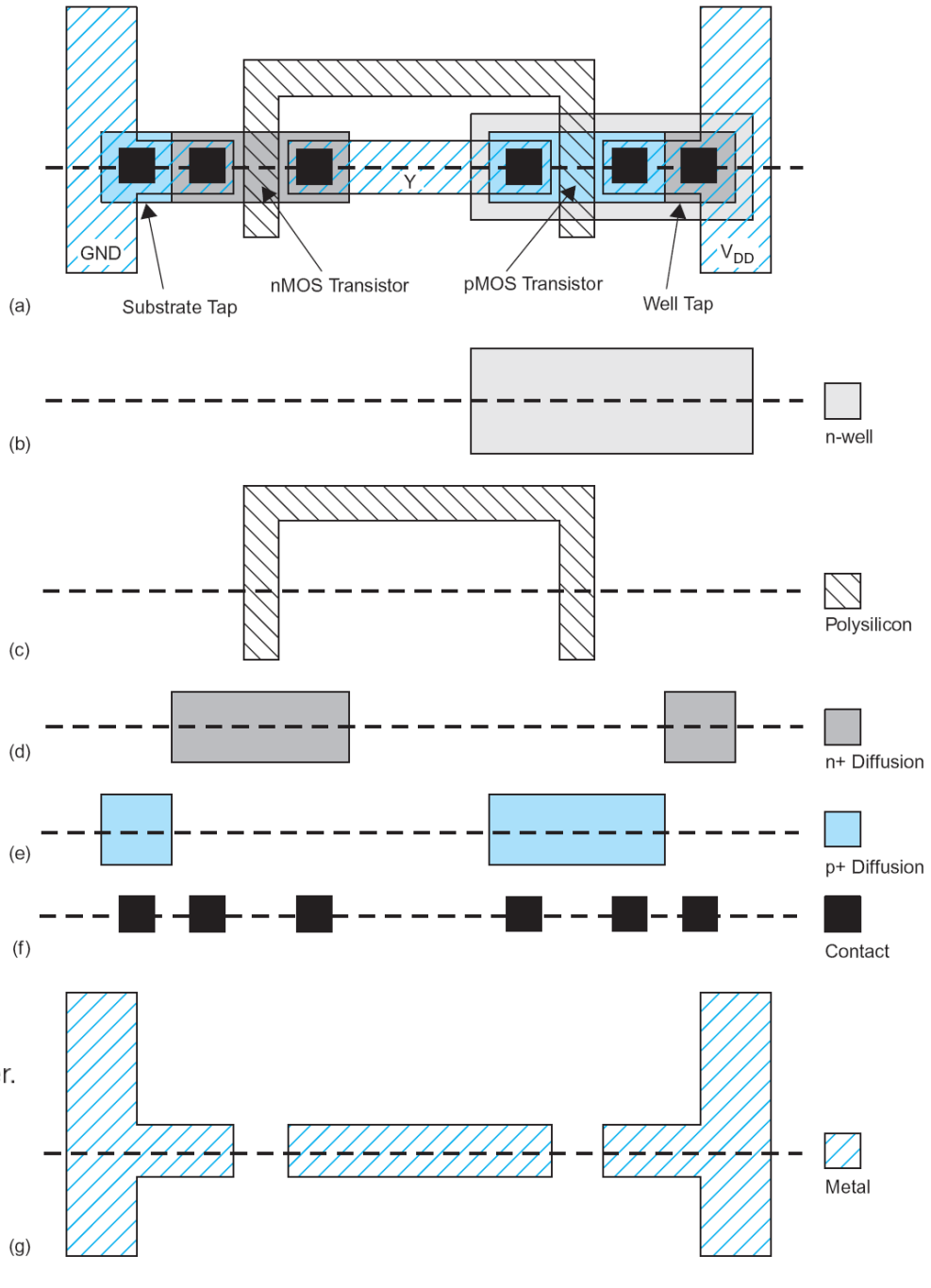

FIGURE 1.35 Inverter mask set. Color version on inside front cover.

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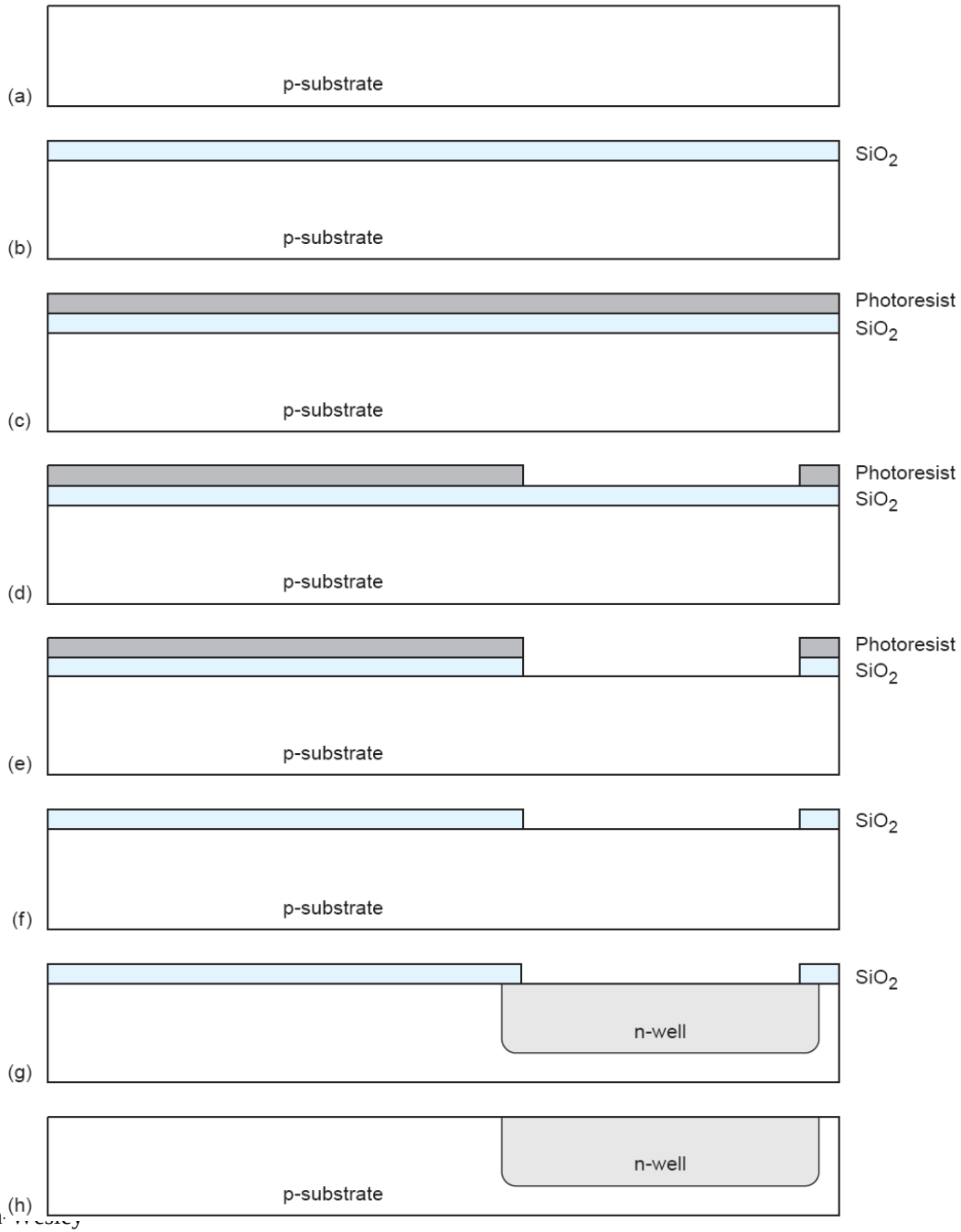

FIGURE 1.36 Cross-sections while manufacturing the n-well

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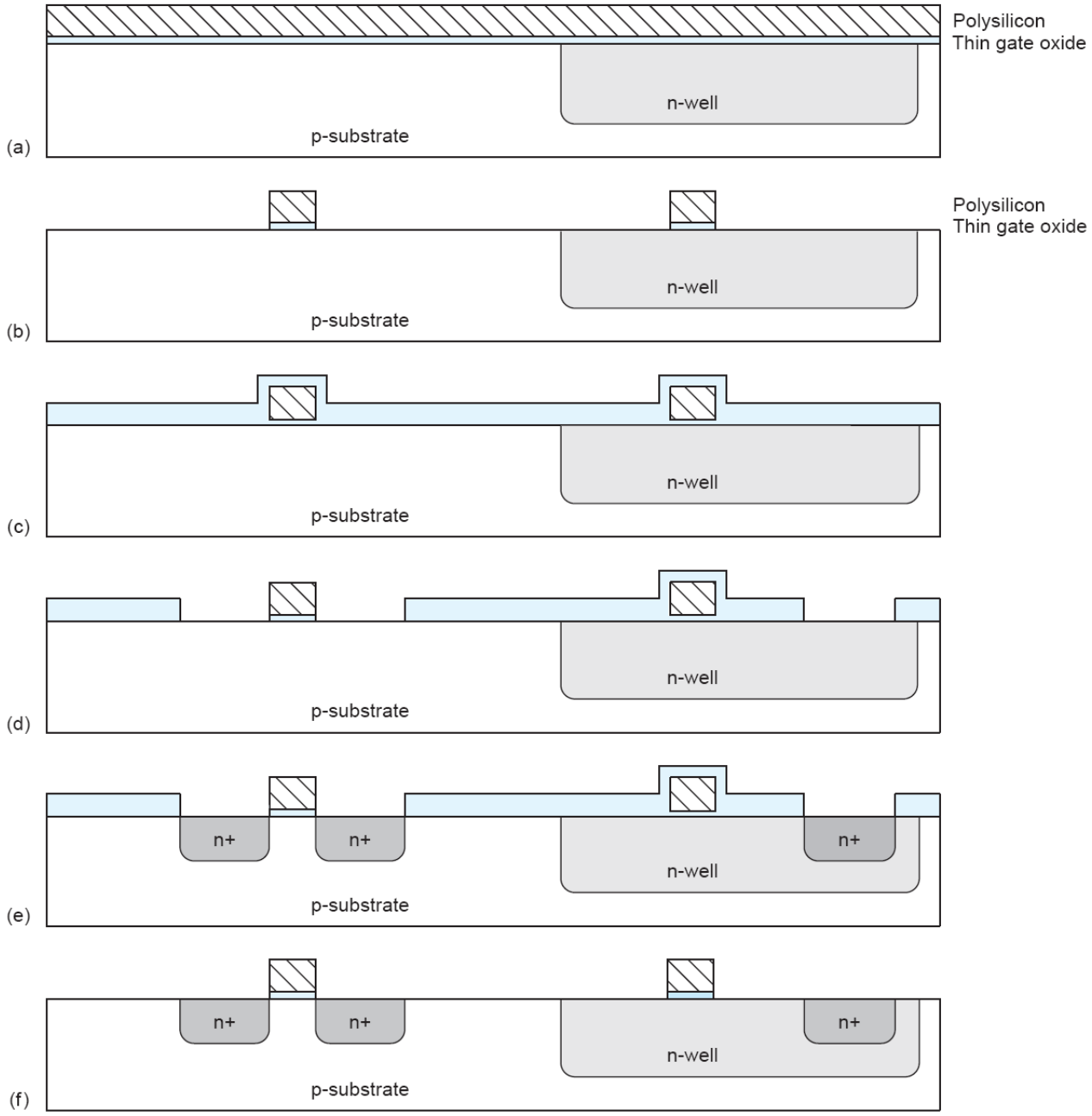

FIGURE 1.37
Cross-sections while manufactuing polysilicon and n-diffusion

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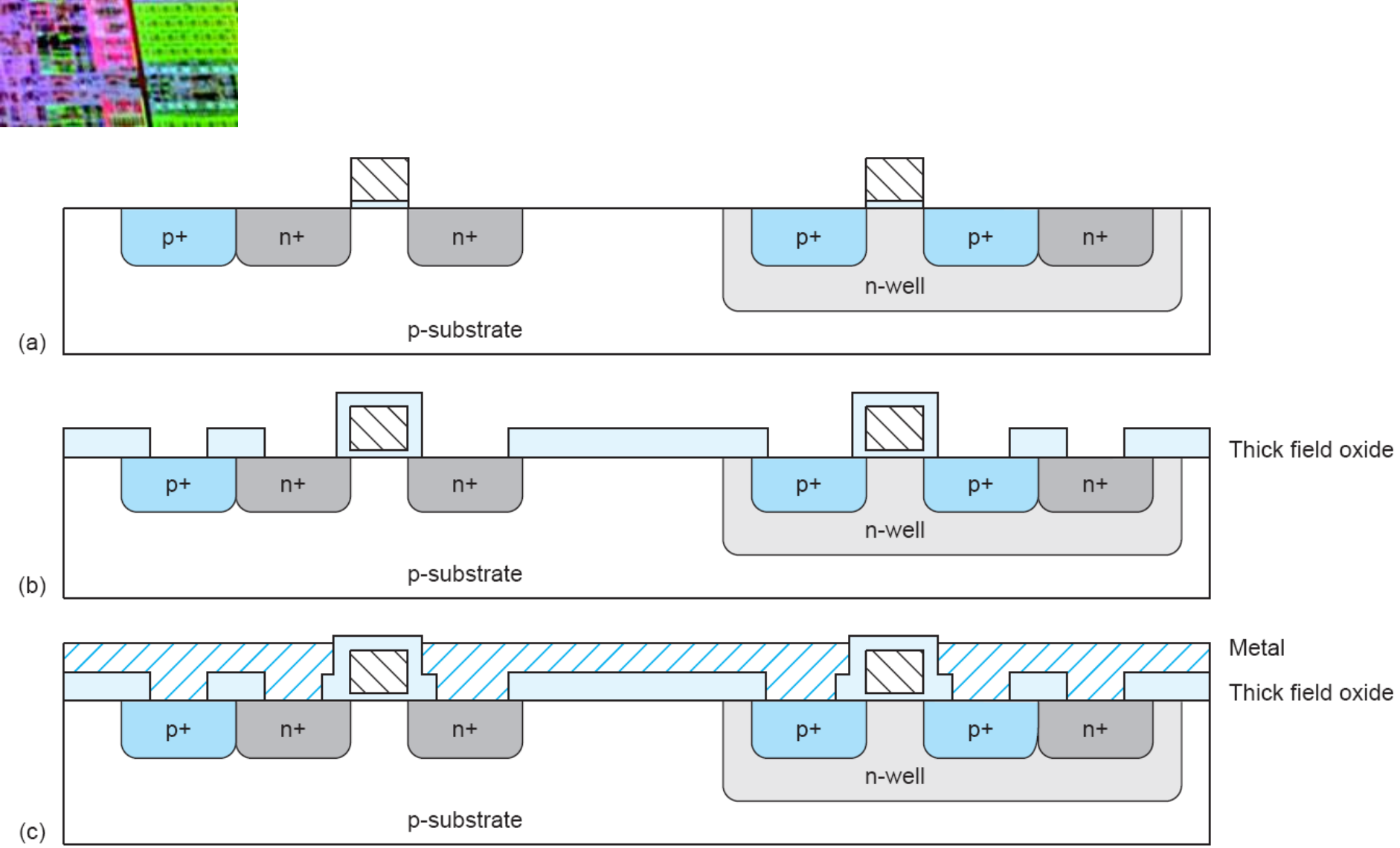

FIGURE 1.38 Cross-sections while manufacturing p-diffusion, contacts, and metal

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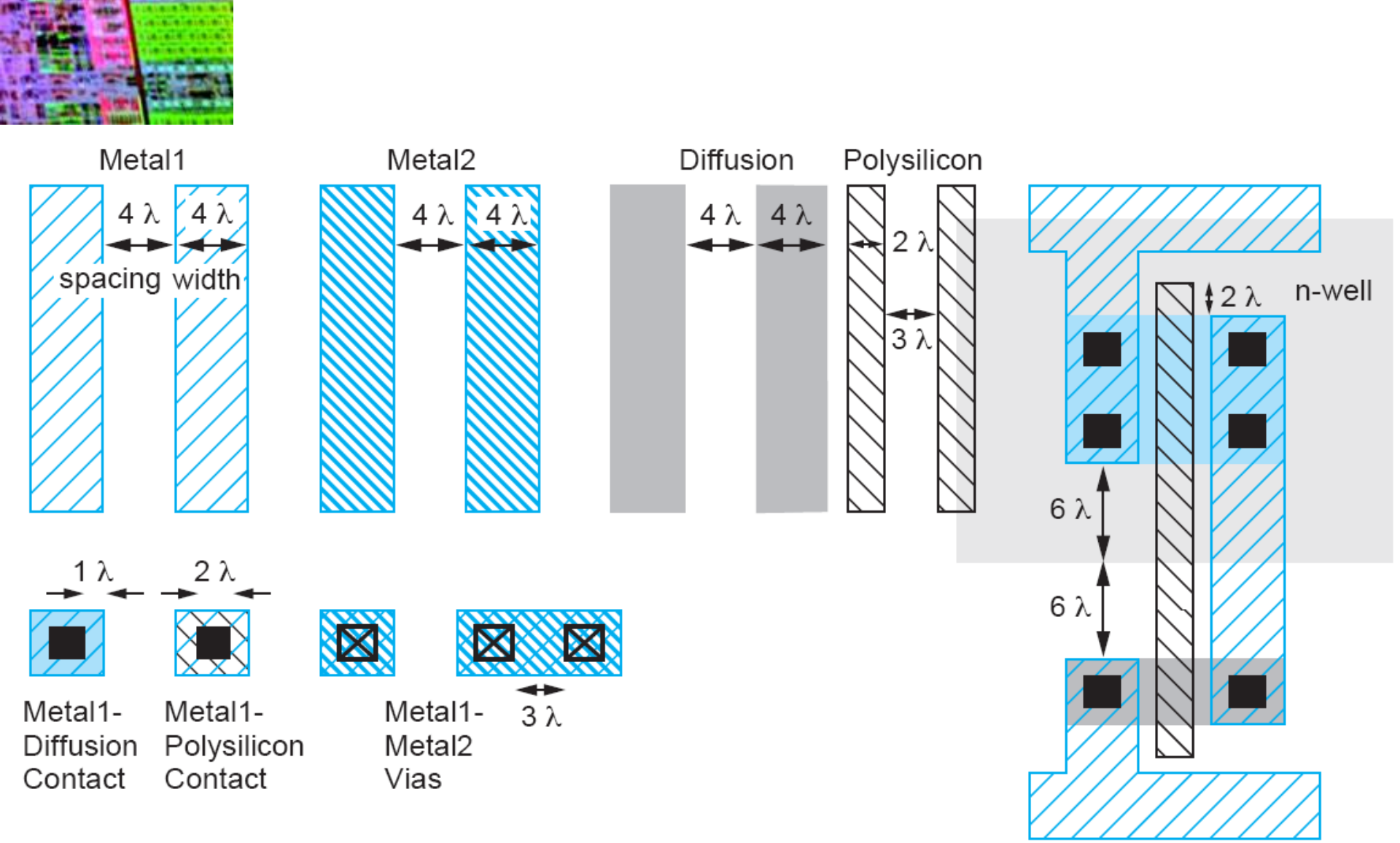

FIGURE 1.39 Simplified λ-based design rules

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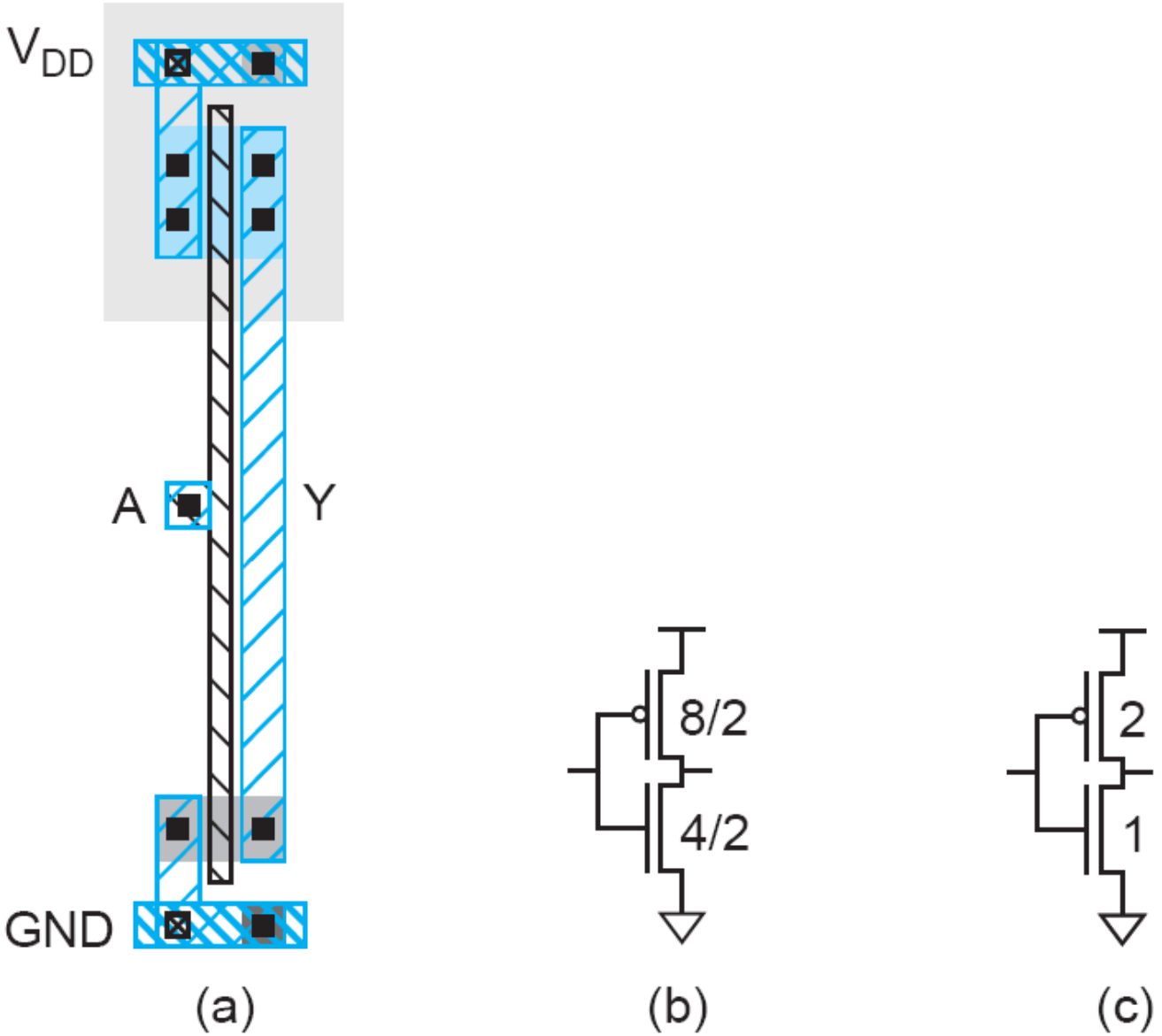

FIGURE 1.40 Inverter with dimensions labeled

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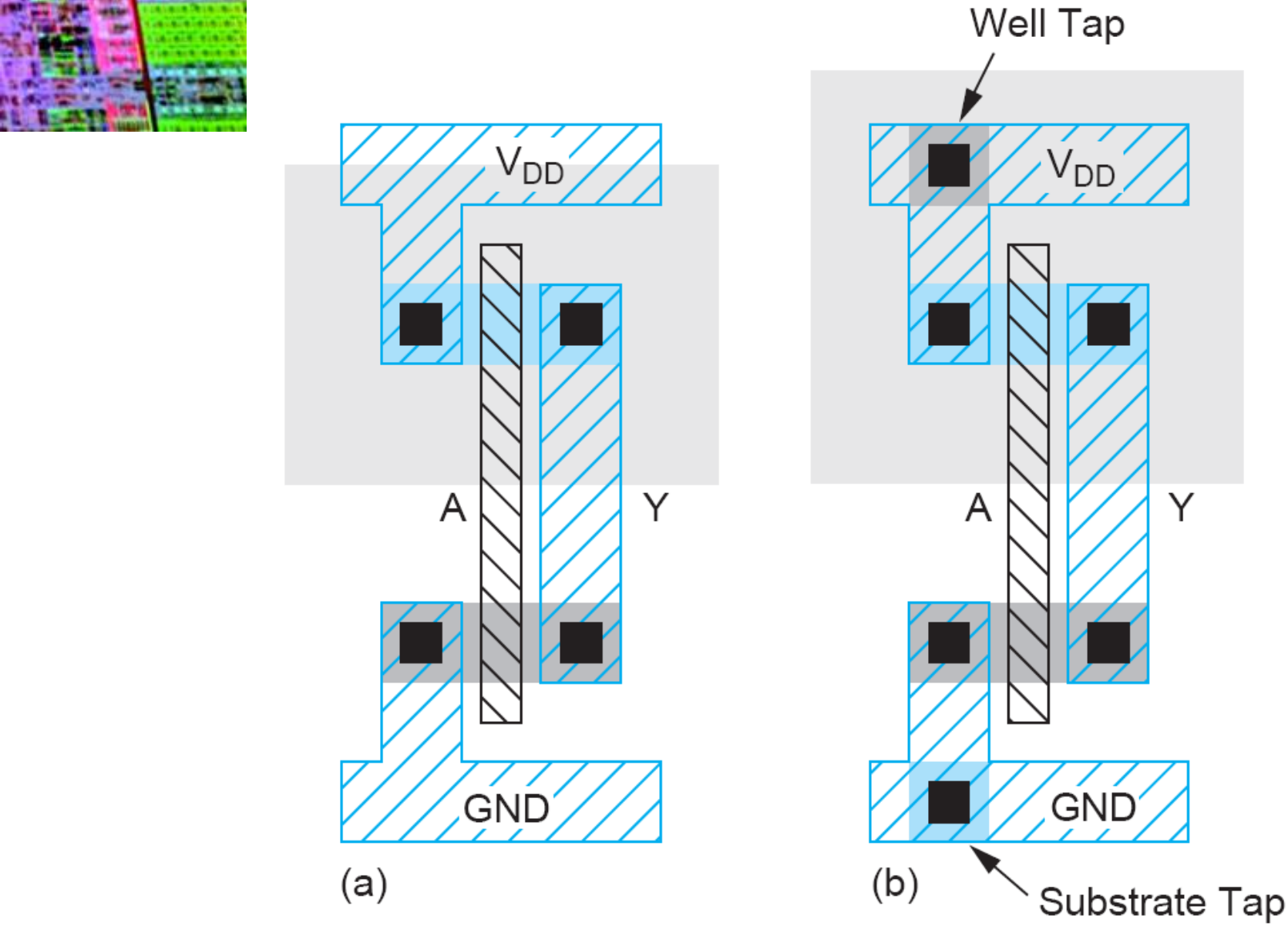

FIGURE 1.41 Inverter cell layout

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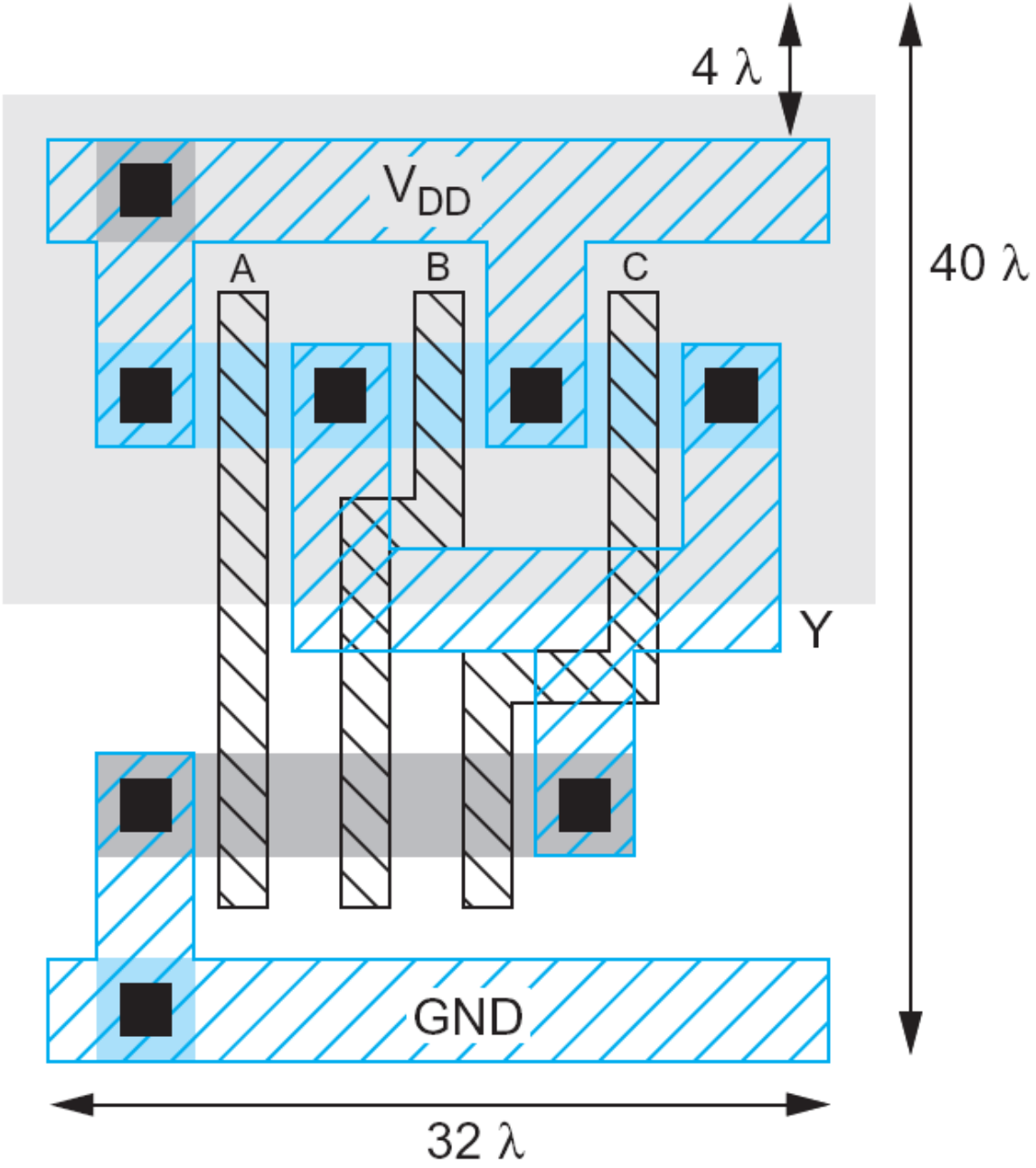

FIGURE 1.42 3-input NAND standard cell gate layouts

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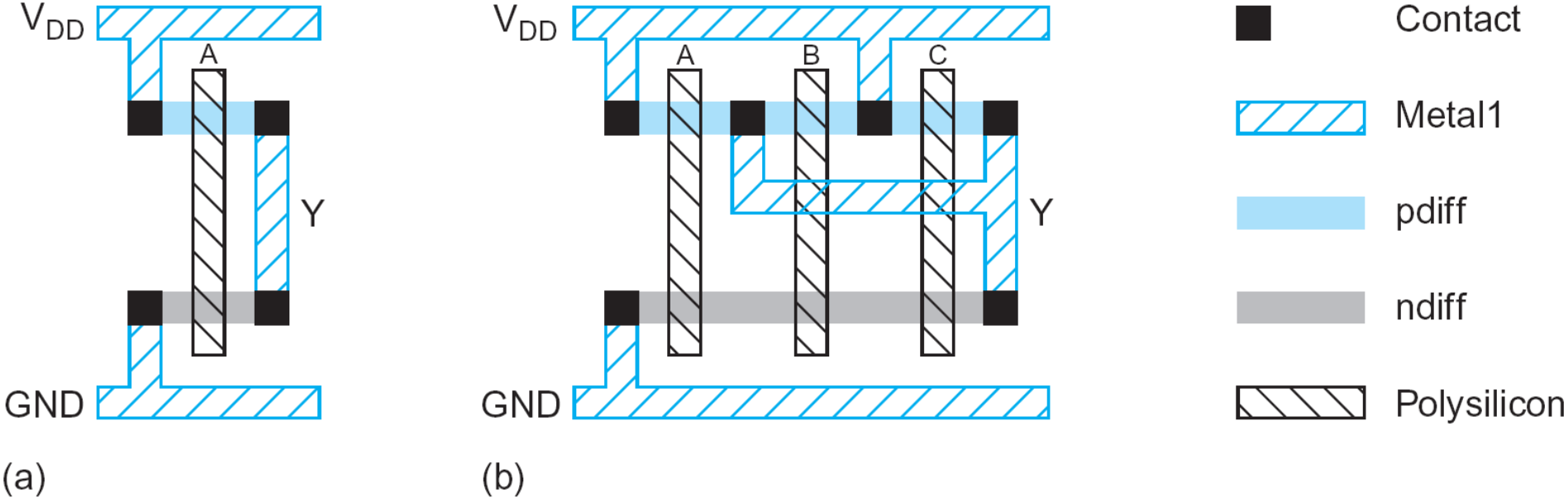

FIGURE 1.43 Stick diagrams of inverter and 3-input NAND gate. Color version on inside front cover.

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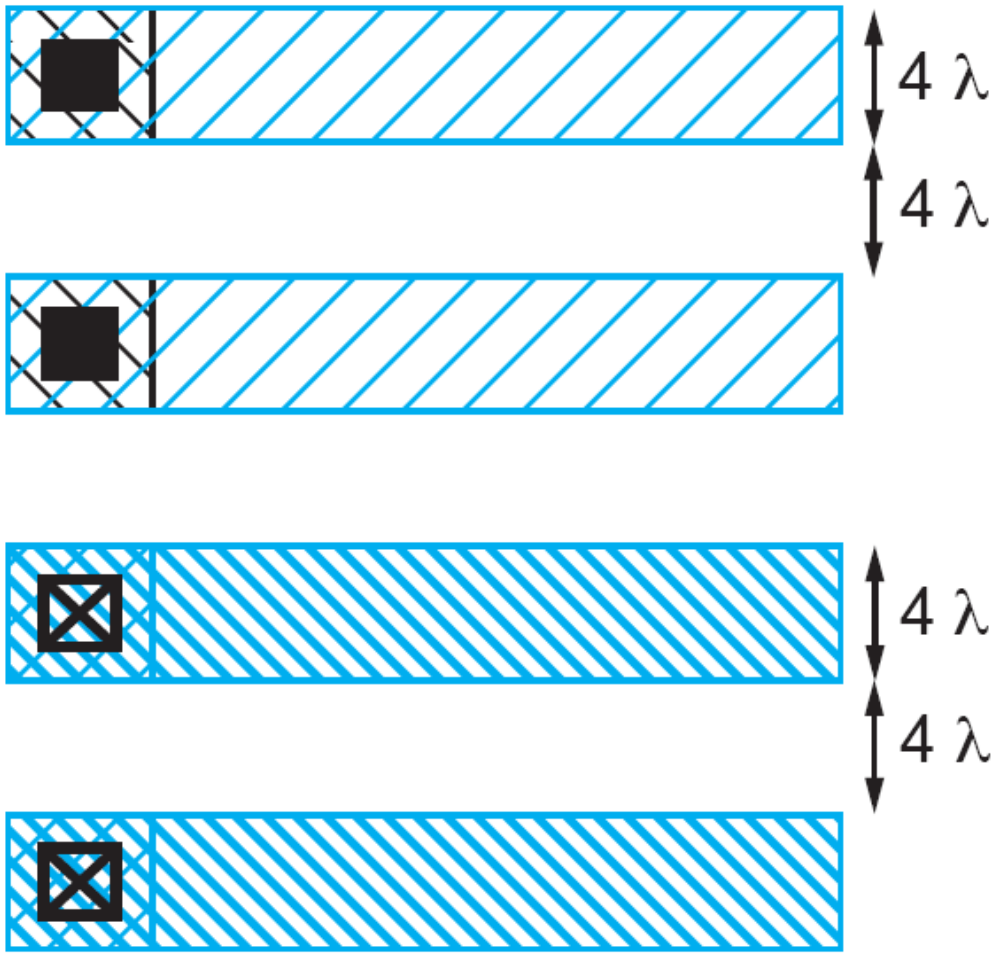

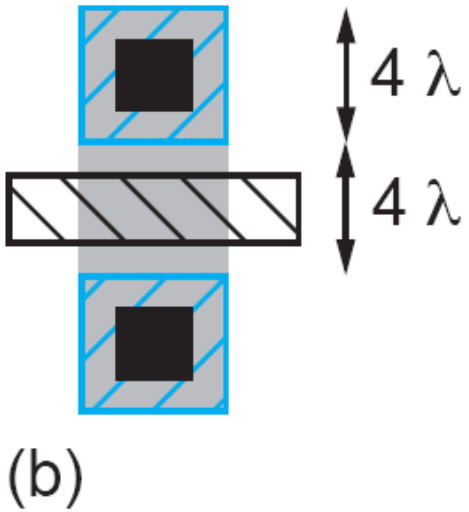

FIGURE 1.44 Pitch of routing tracks

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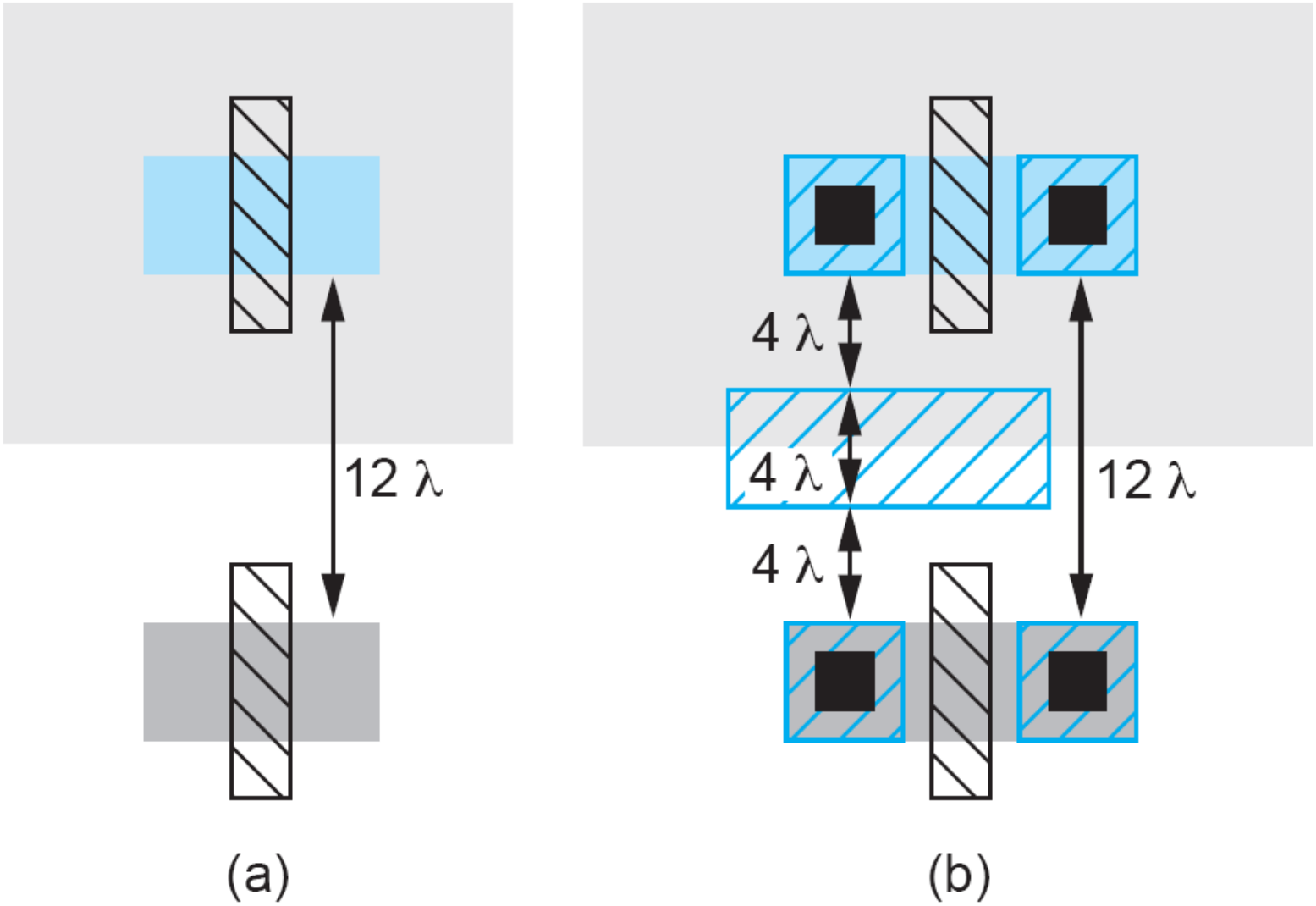
FIGURE 1.45 Spacing between nMOS and pMOS transistors



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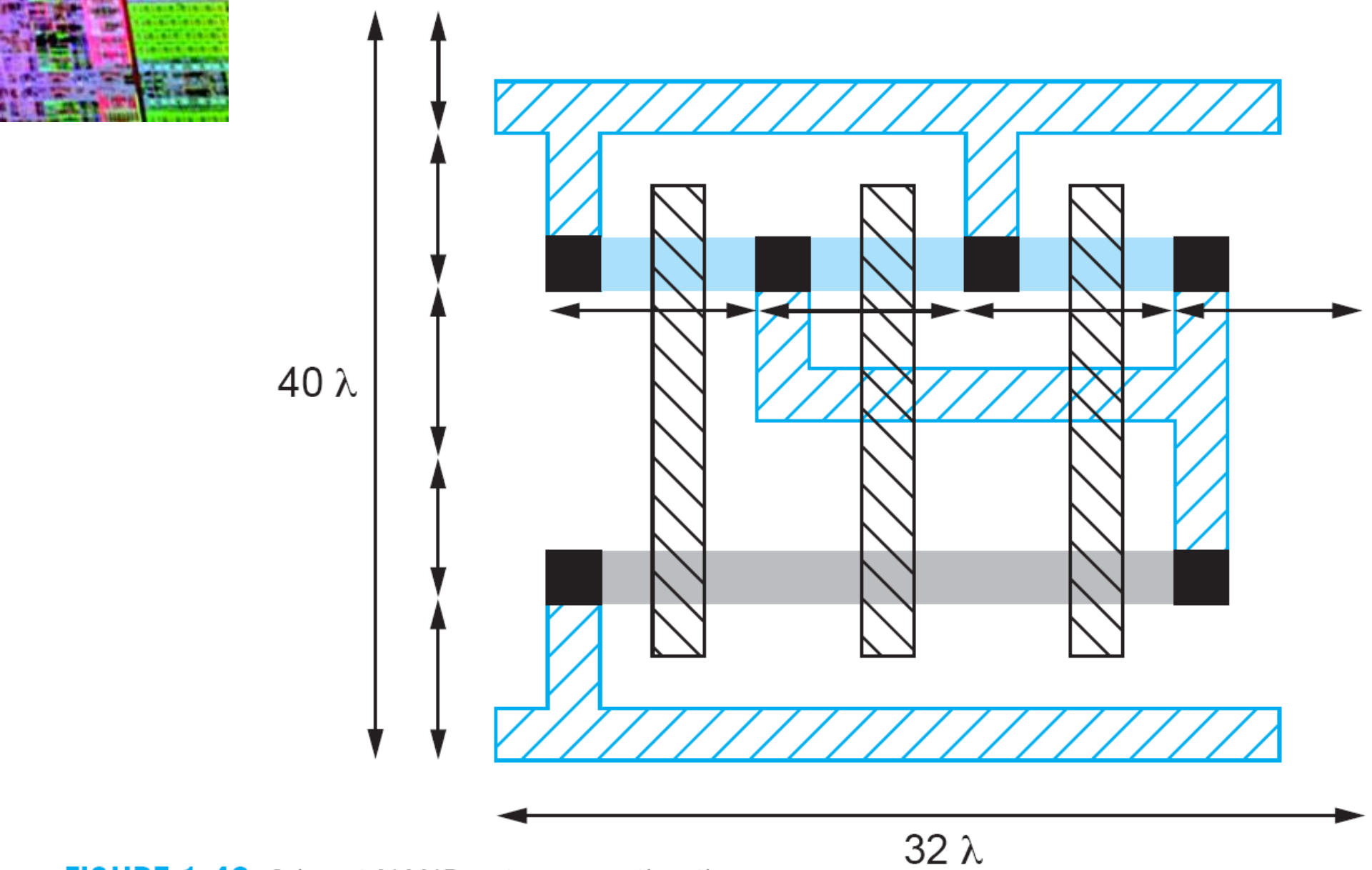

FIGURE 1.46 3-input NAND gate area estimation

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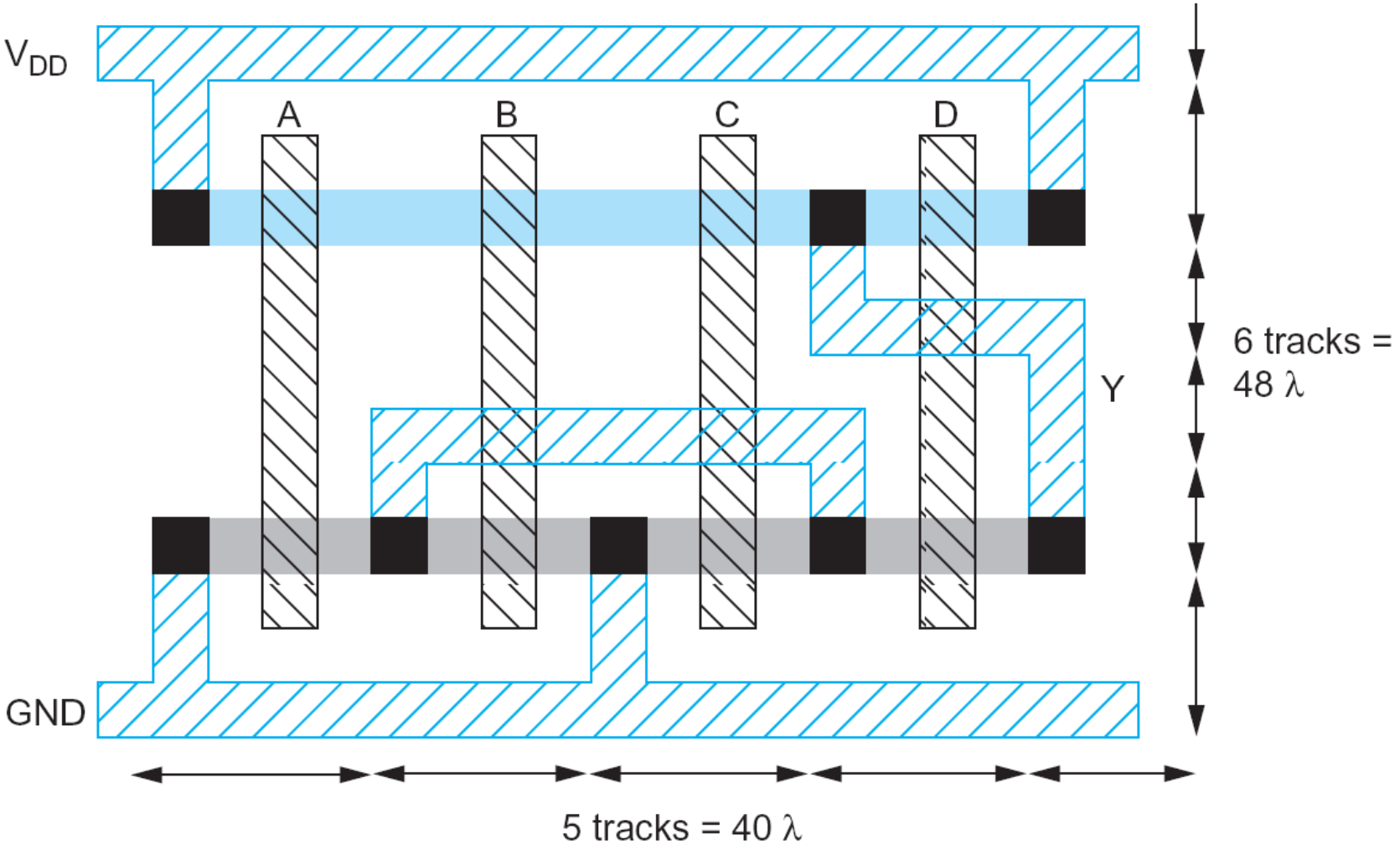

FIGURE 1.47 CMOS compound gate for function $Y = \overline{(A + B + C) \bullet D}$

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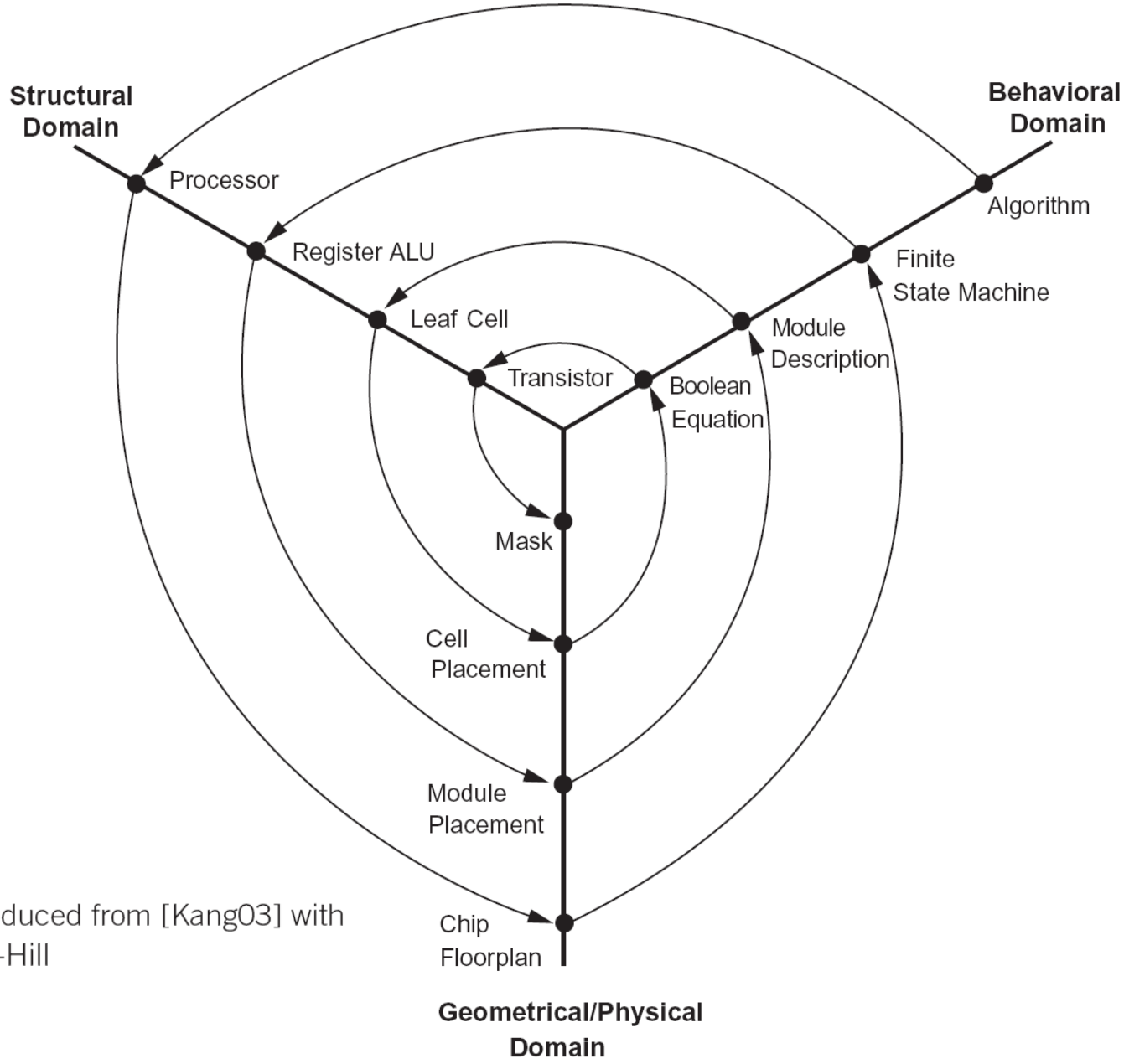

FIGURE 1.48 Y Diagram. Reproduced from [Kang03] with with permission of The McGraw-Hill Companies.

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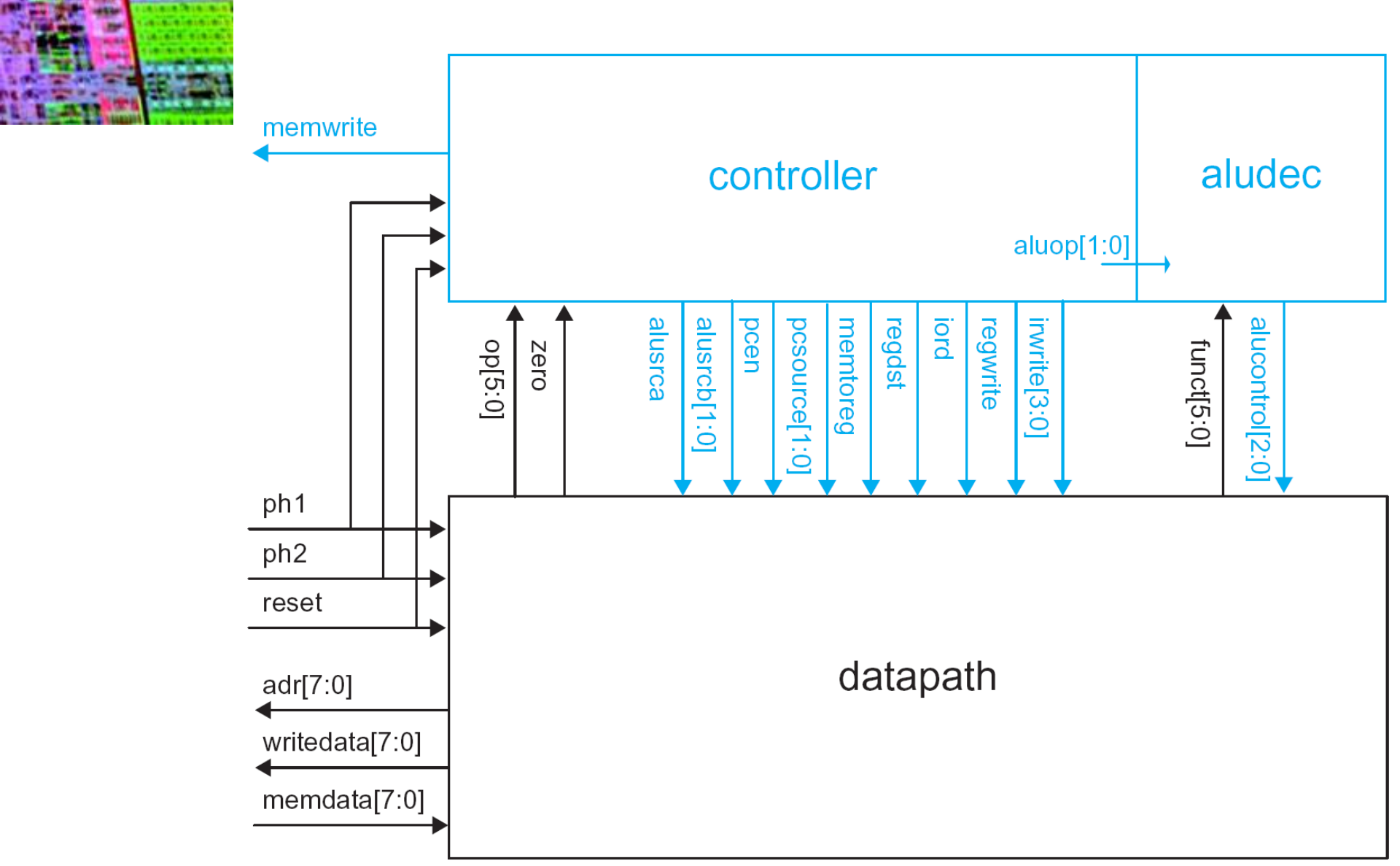

FIGURE 1.56 Top-level MIPS block diagram

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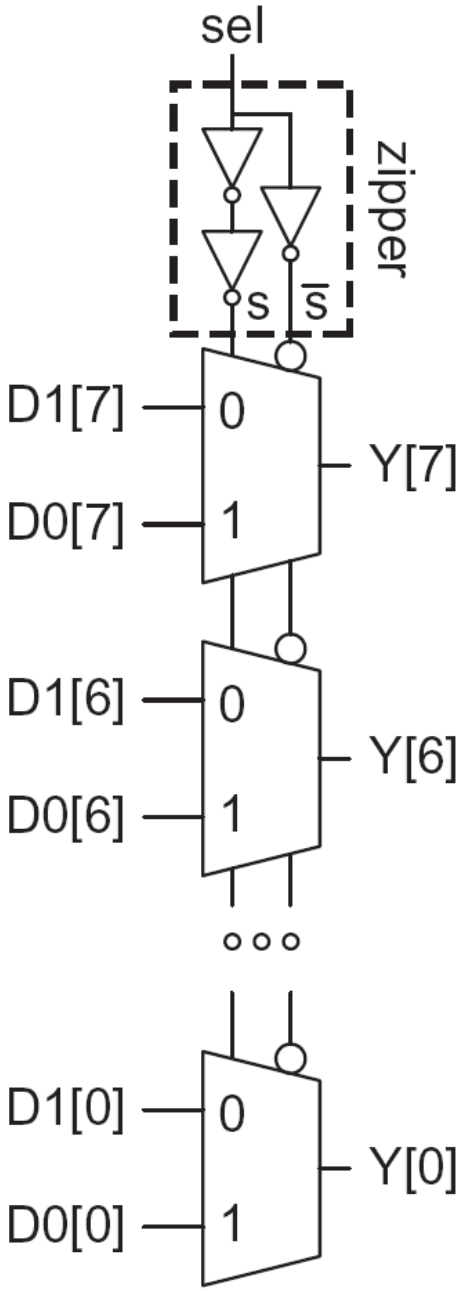

FIGURE 1.57 8-bit 2:1 multiplexer wordslice

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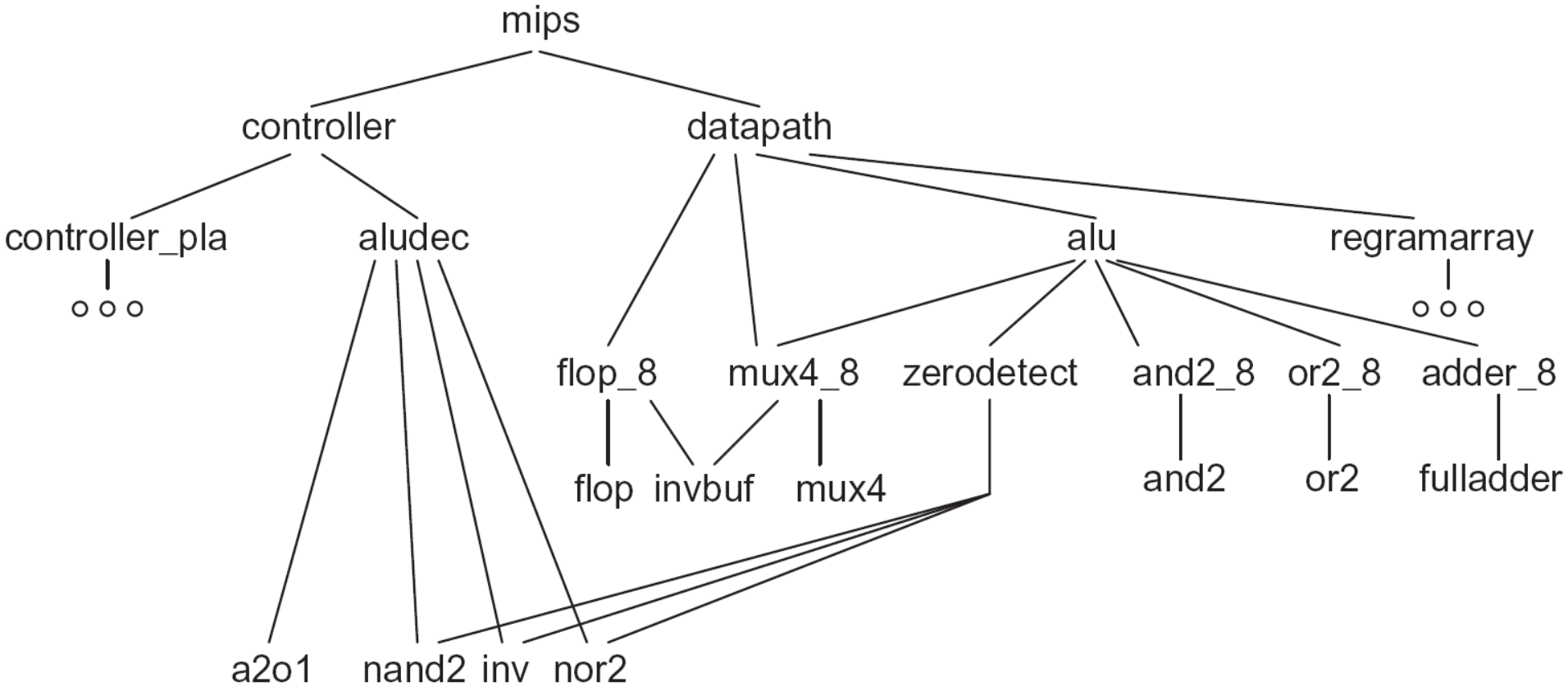

FIGURE 1.58 MIPS design hierarchy

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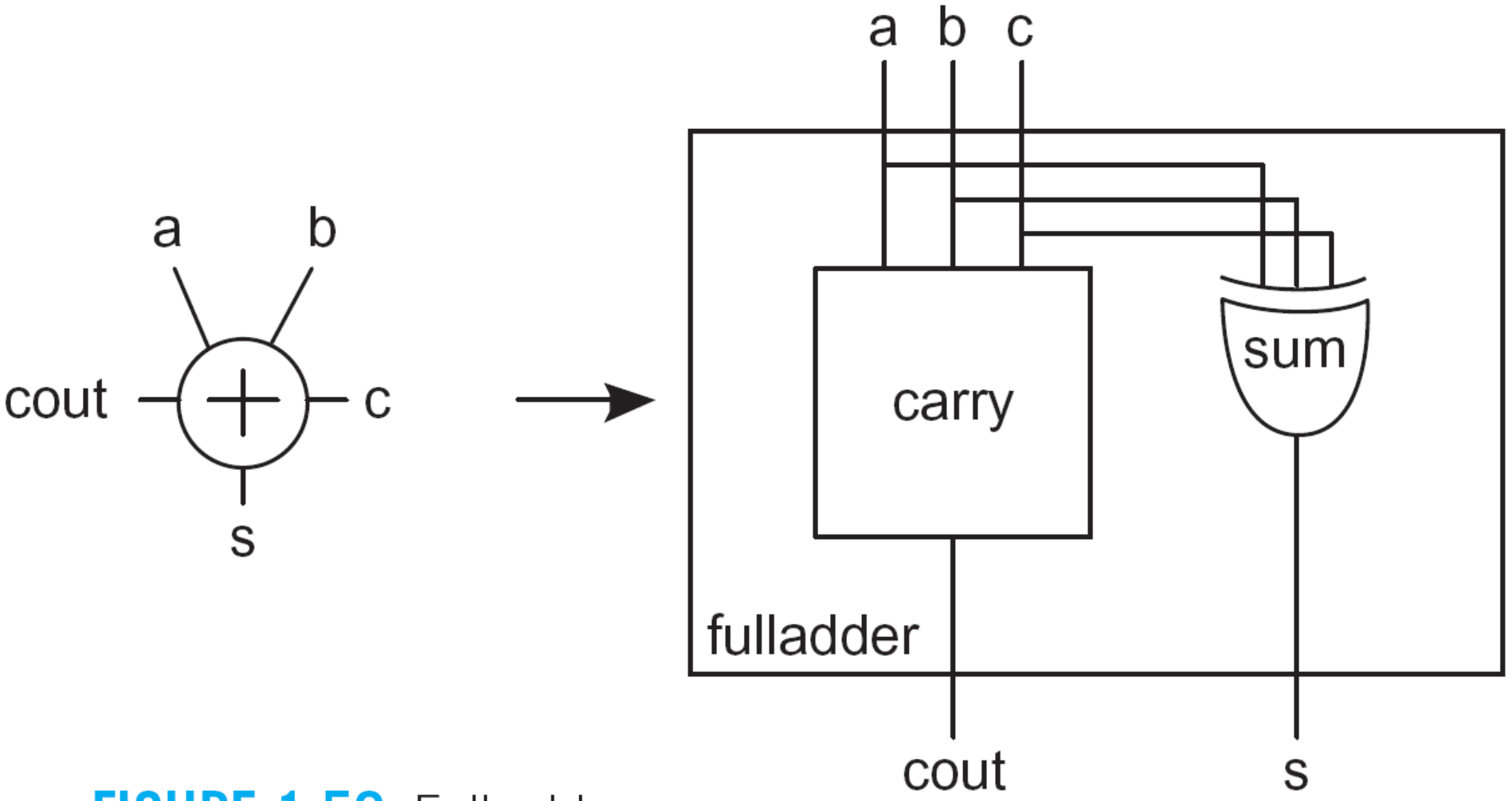

FIGURE 1.59 Full adder

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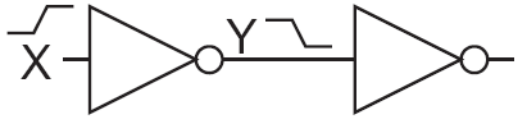
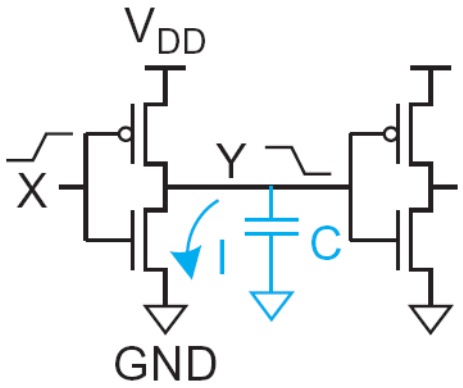
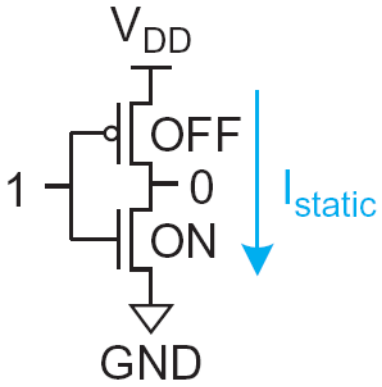


(a)



(b)



(c)

FIGURE 1.60 Circuit delay and power: (a) inverter pair, (b) transistor-level model showing capacitance and current during switching, (c) static leakage current during quiescent operation

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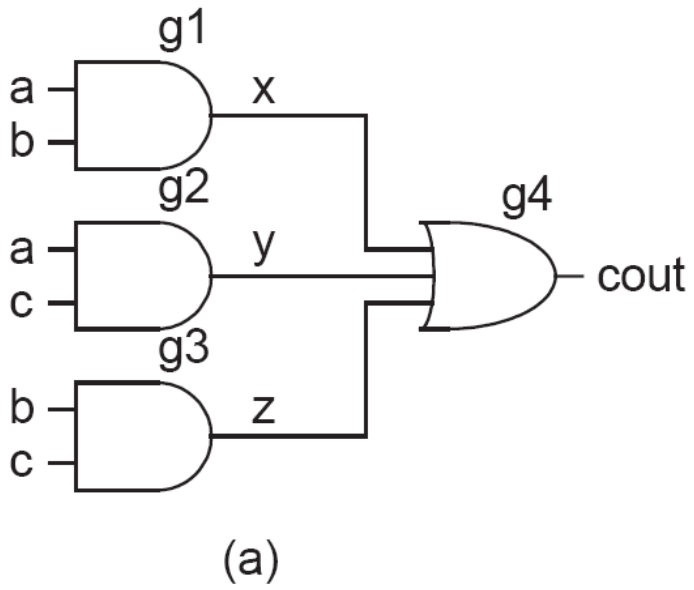
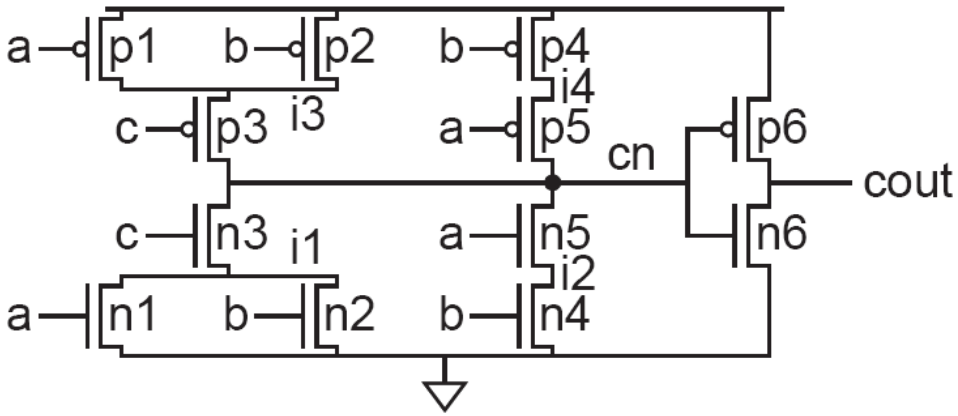


(a)



(b)

FIGURE 1.61 Carry subcircuit

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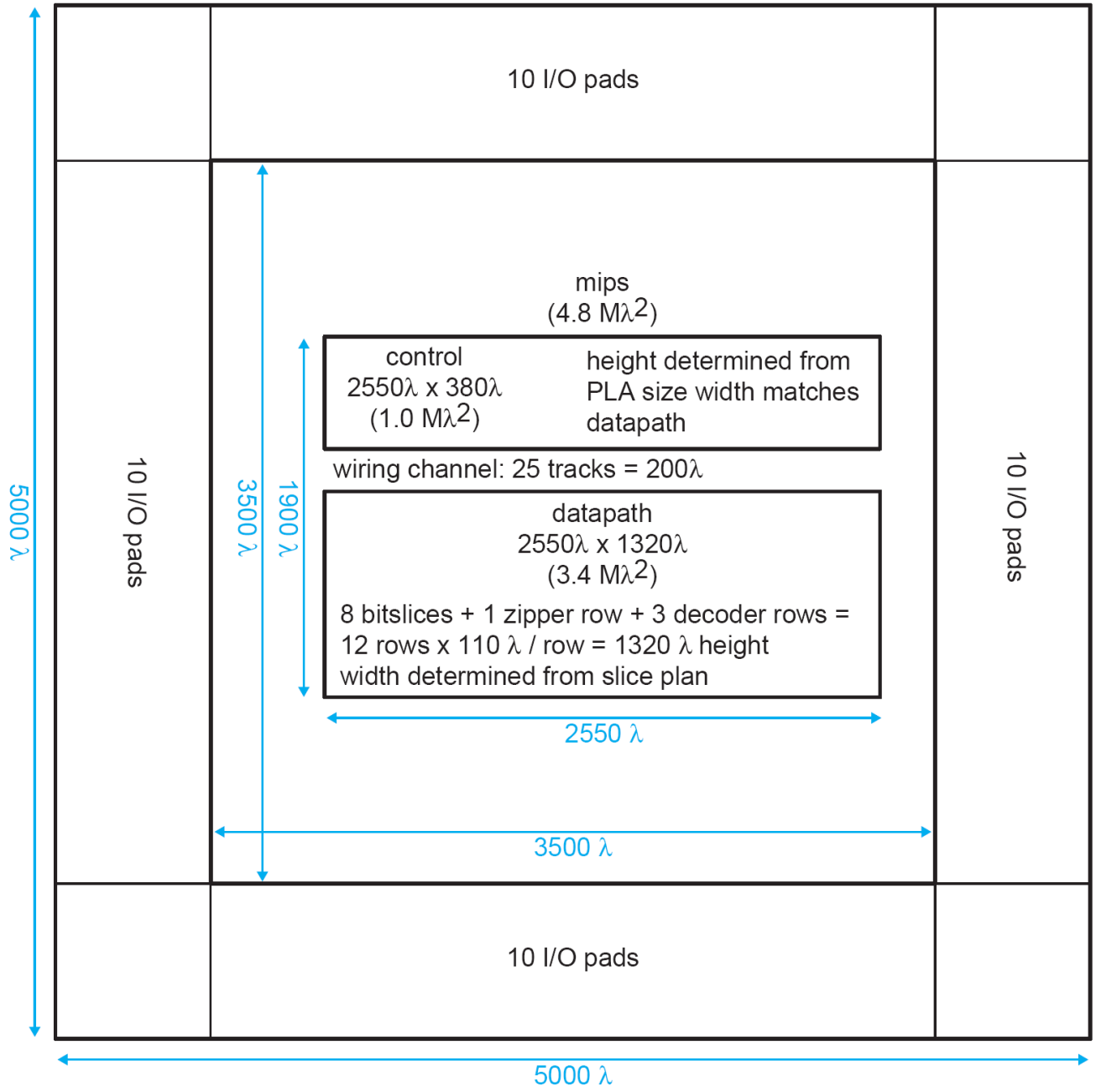

FIGURE 1.62 MIPS floorplan

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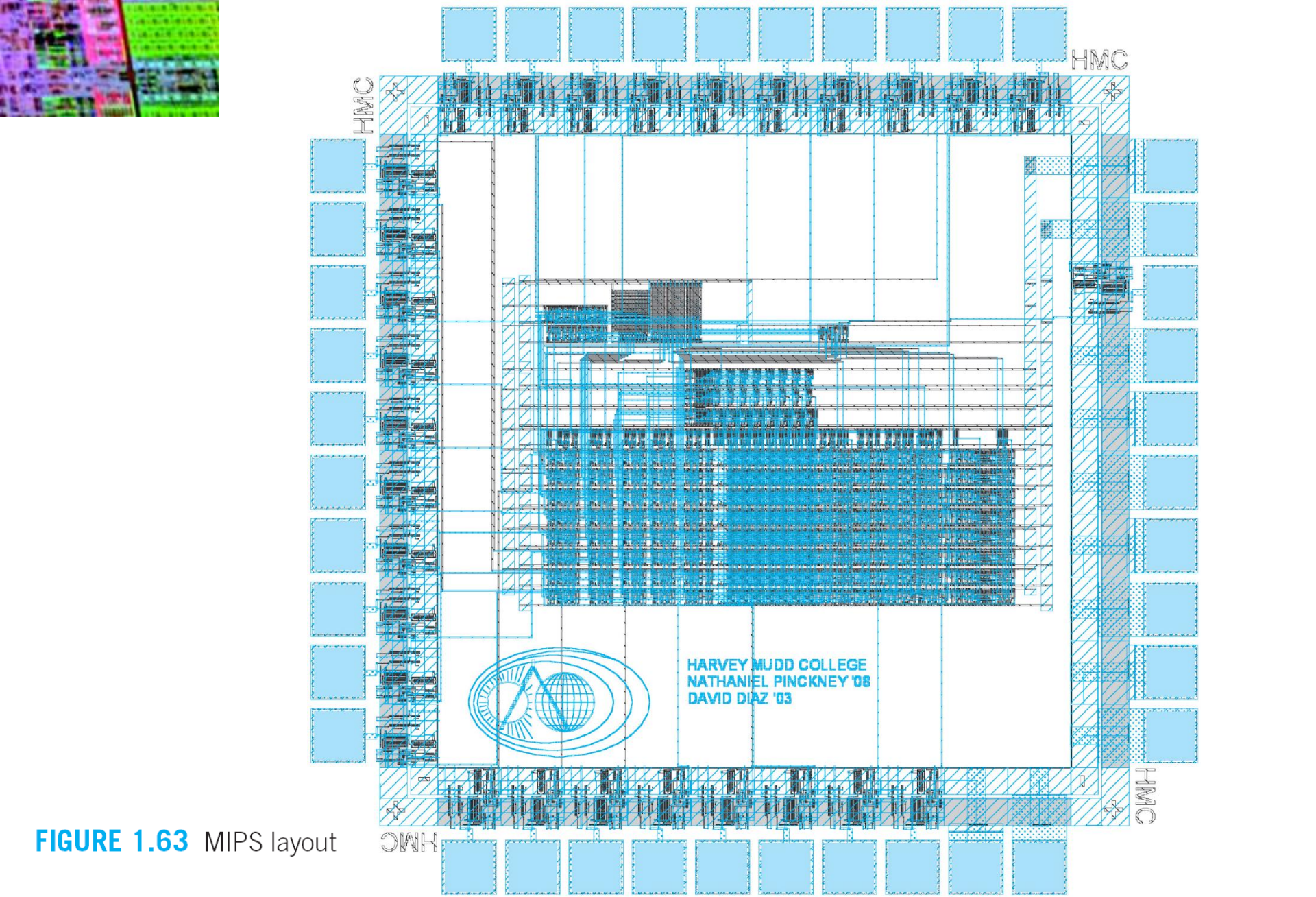

FIGURE 1.63 MIPS layout

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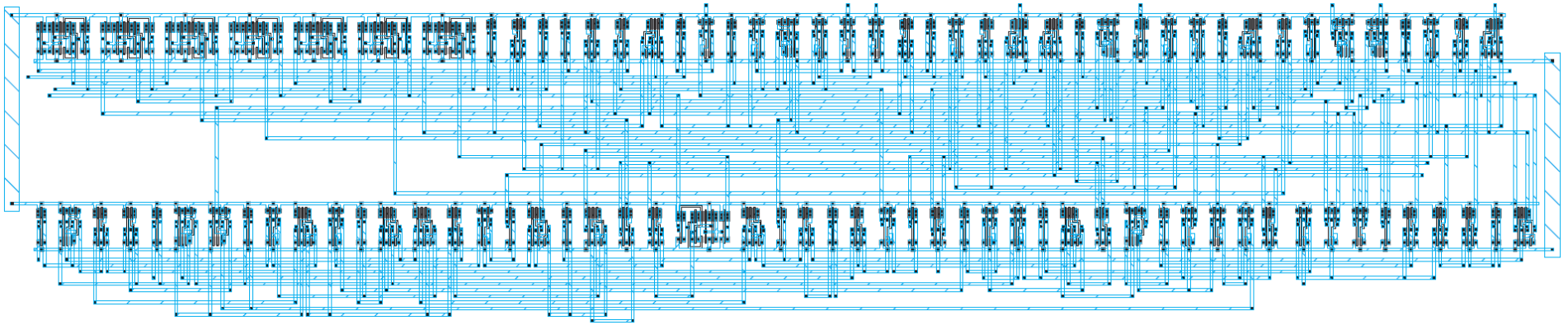

FIGURE 1.64 MIPS controller layout (synthesized)

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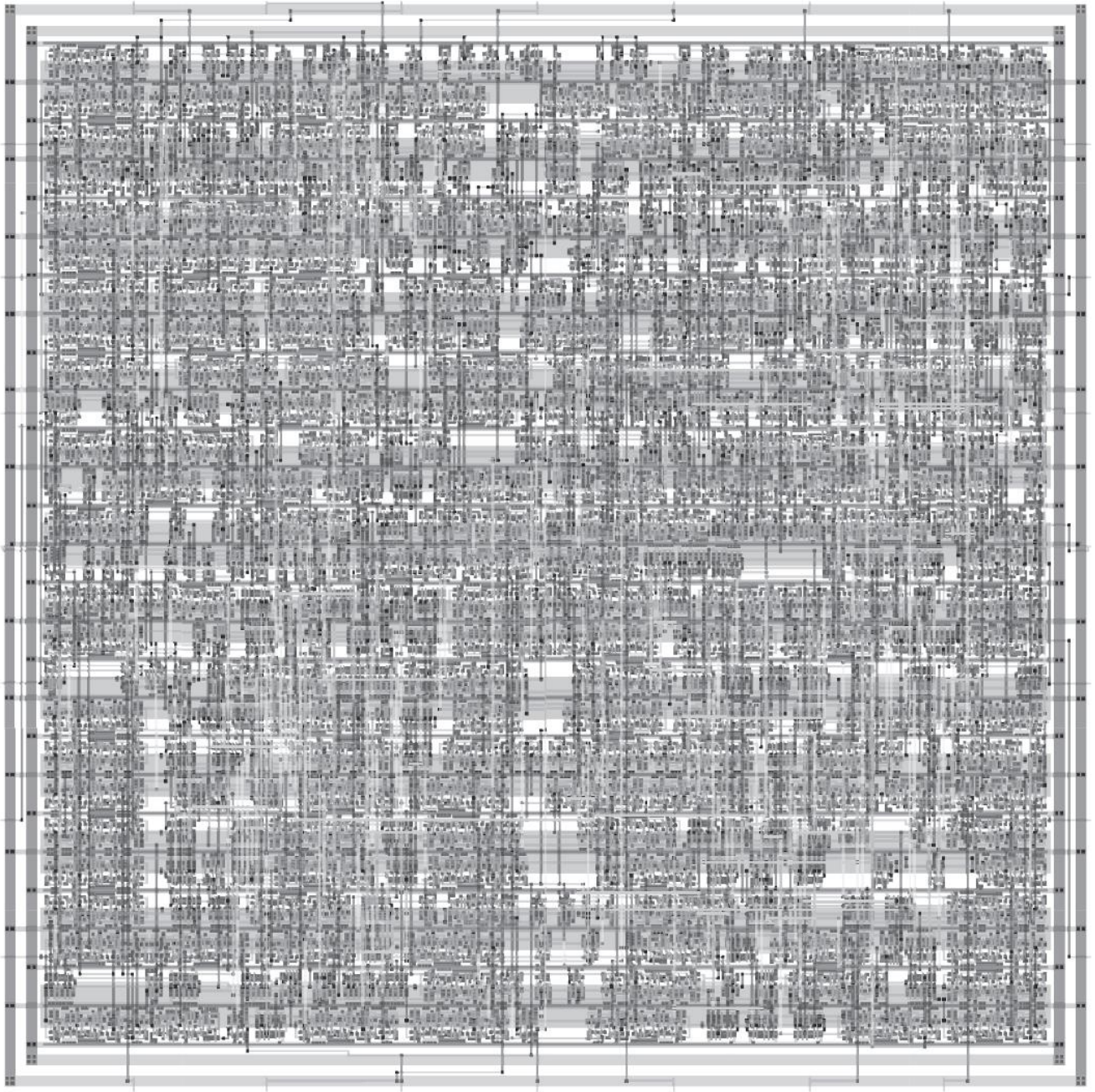

FIGURE 1.65 Synthesized MIPS processor

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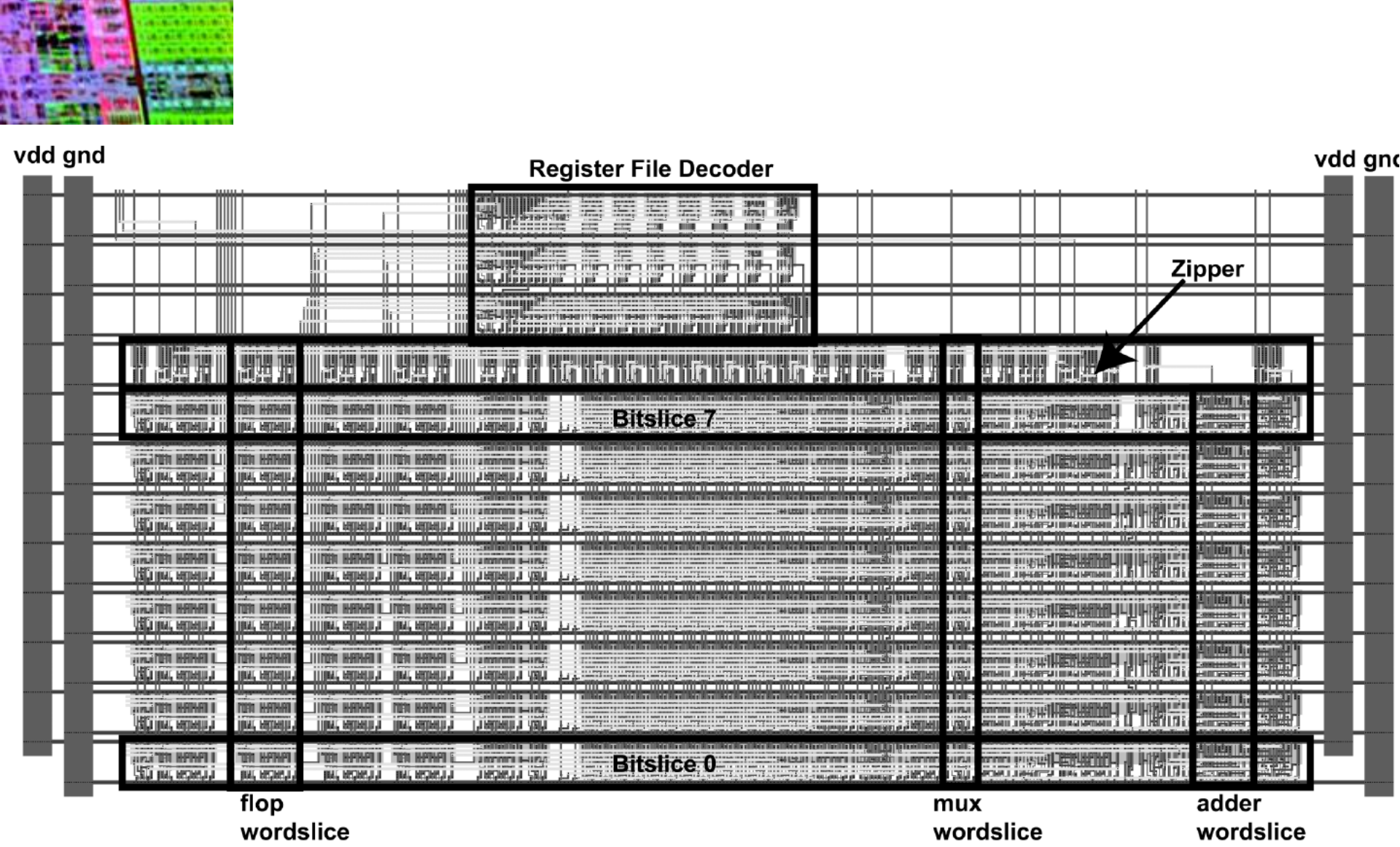

FIGURE 1.67 MIPS datapath layout

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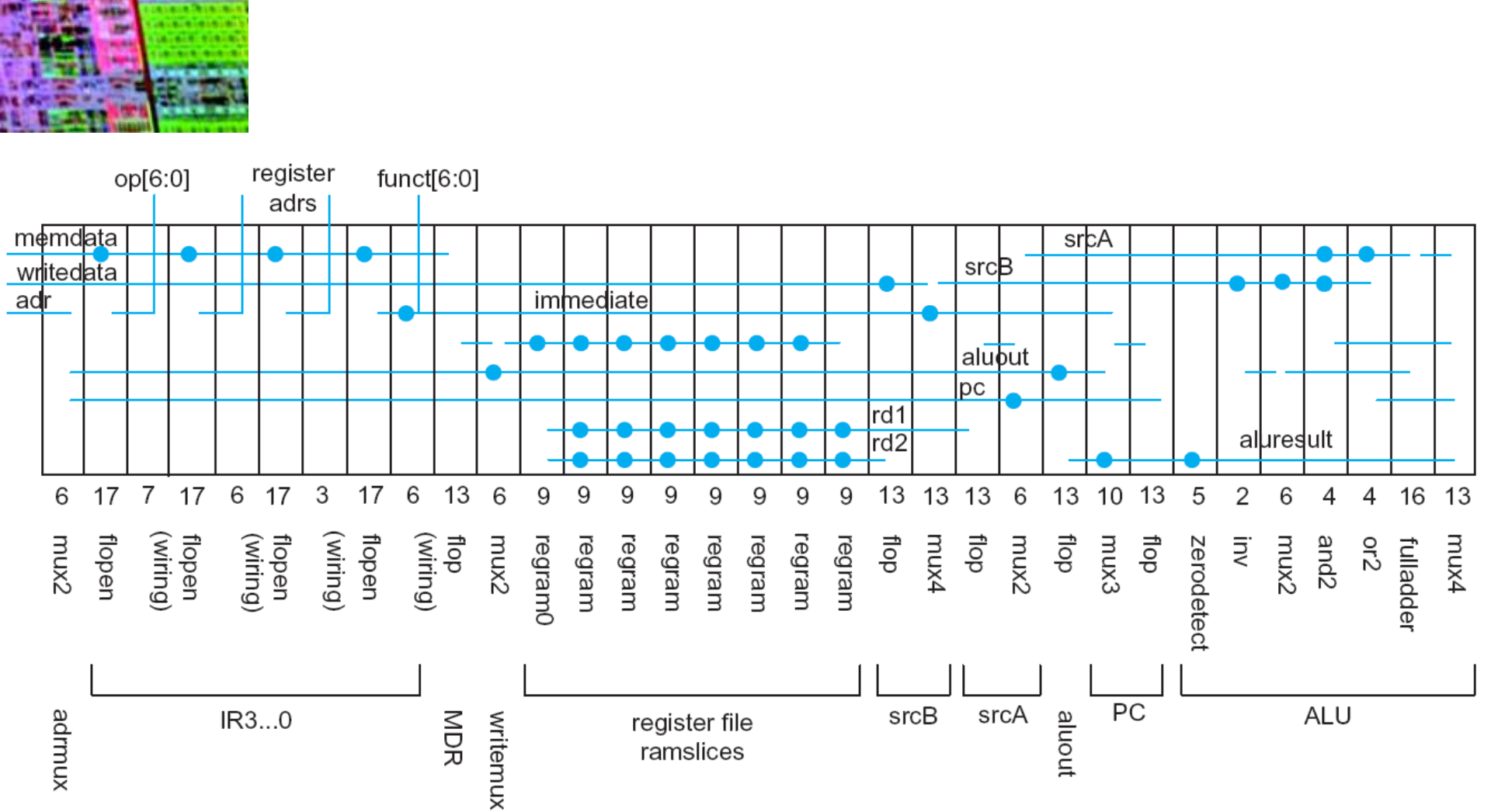

FIGURE 1.68 Datapath slice plan

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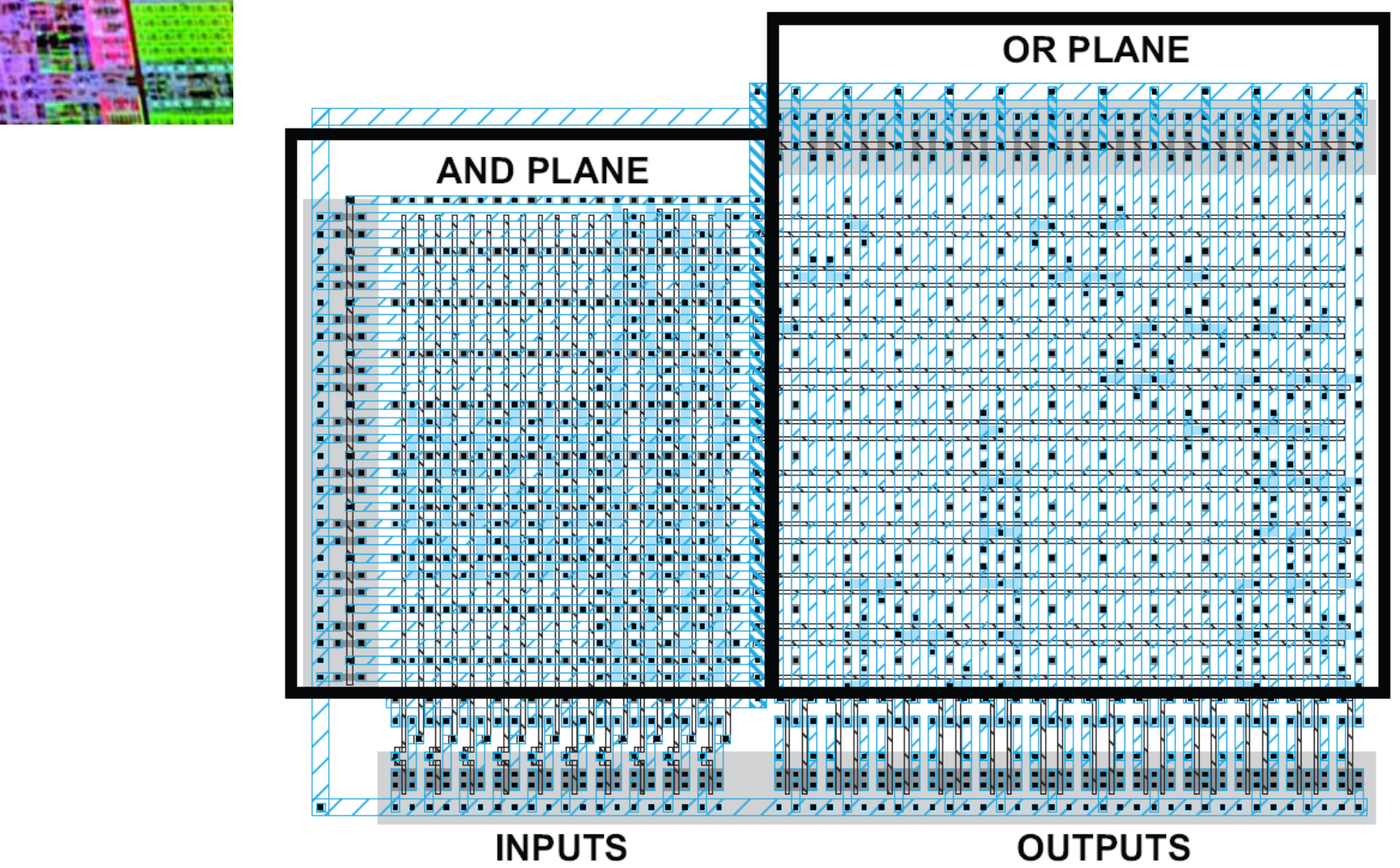

FIGURE 1.69 PLA for control FSM

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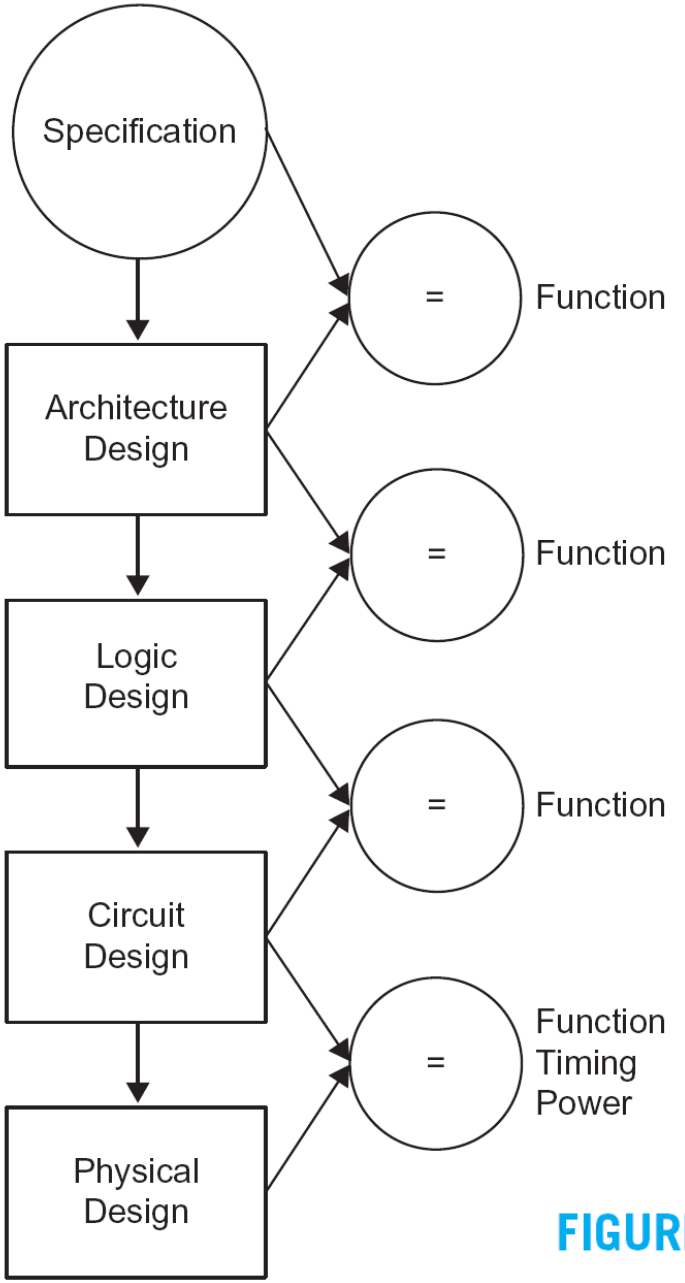

FIGURE 1.70 Design and verification sequence

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FIGURE 1.71 Engineer holding processed 12-inch wafer. Photograph courtesy of the Intel Corporation.

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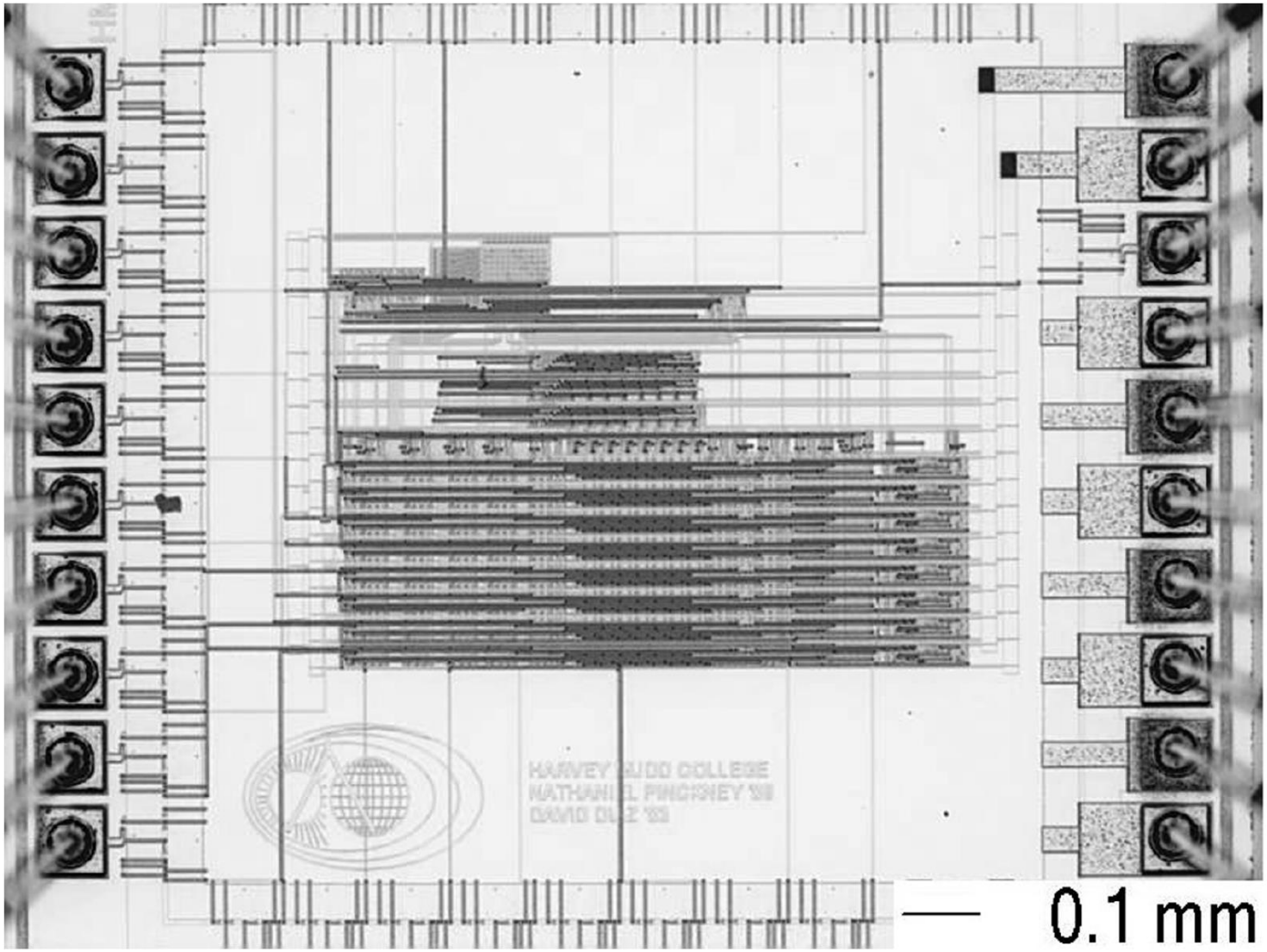

FIGURE 1.72 MIPS processor photomicrograph (only part of pad frame shown)

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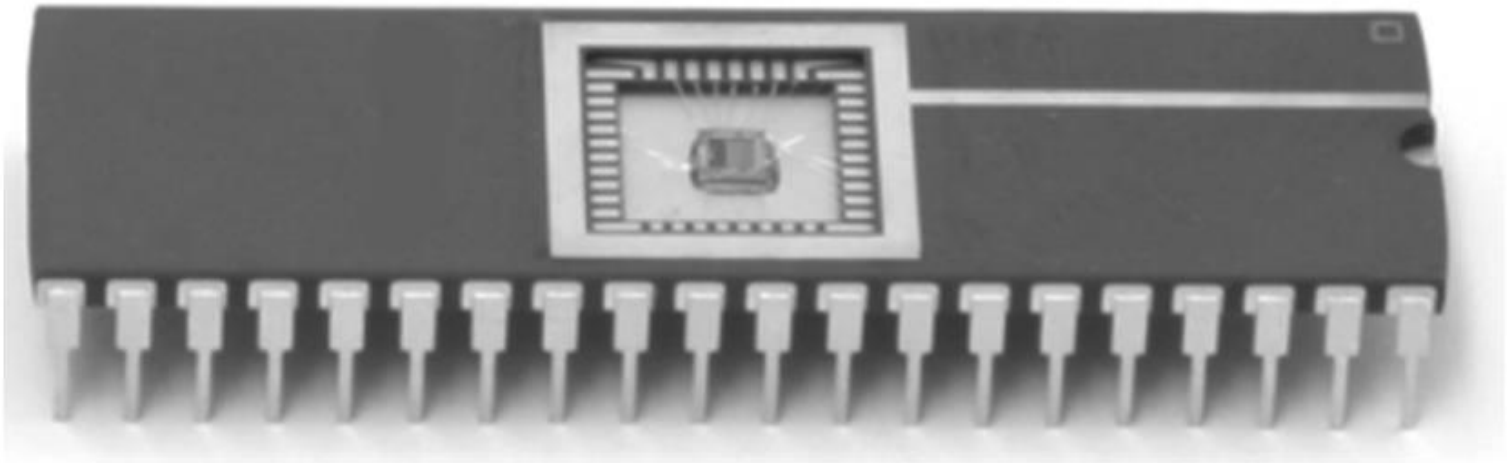

FIGURE 1.73 Chip in a 40-pin dual-inline package

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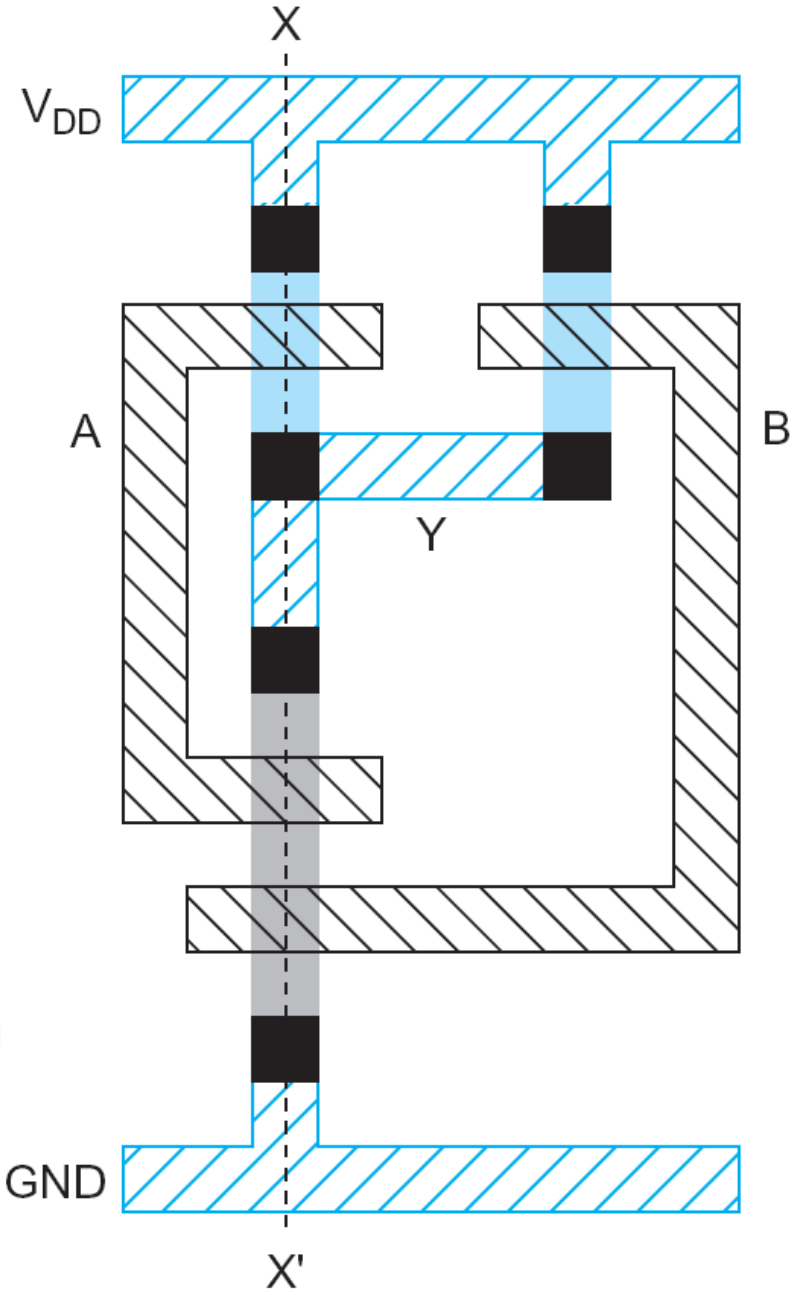

FIGURE 1.74 2-input NAND gate stick diagram

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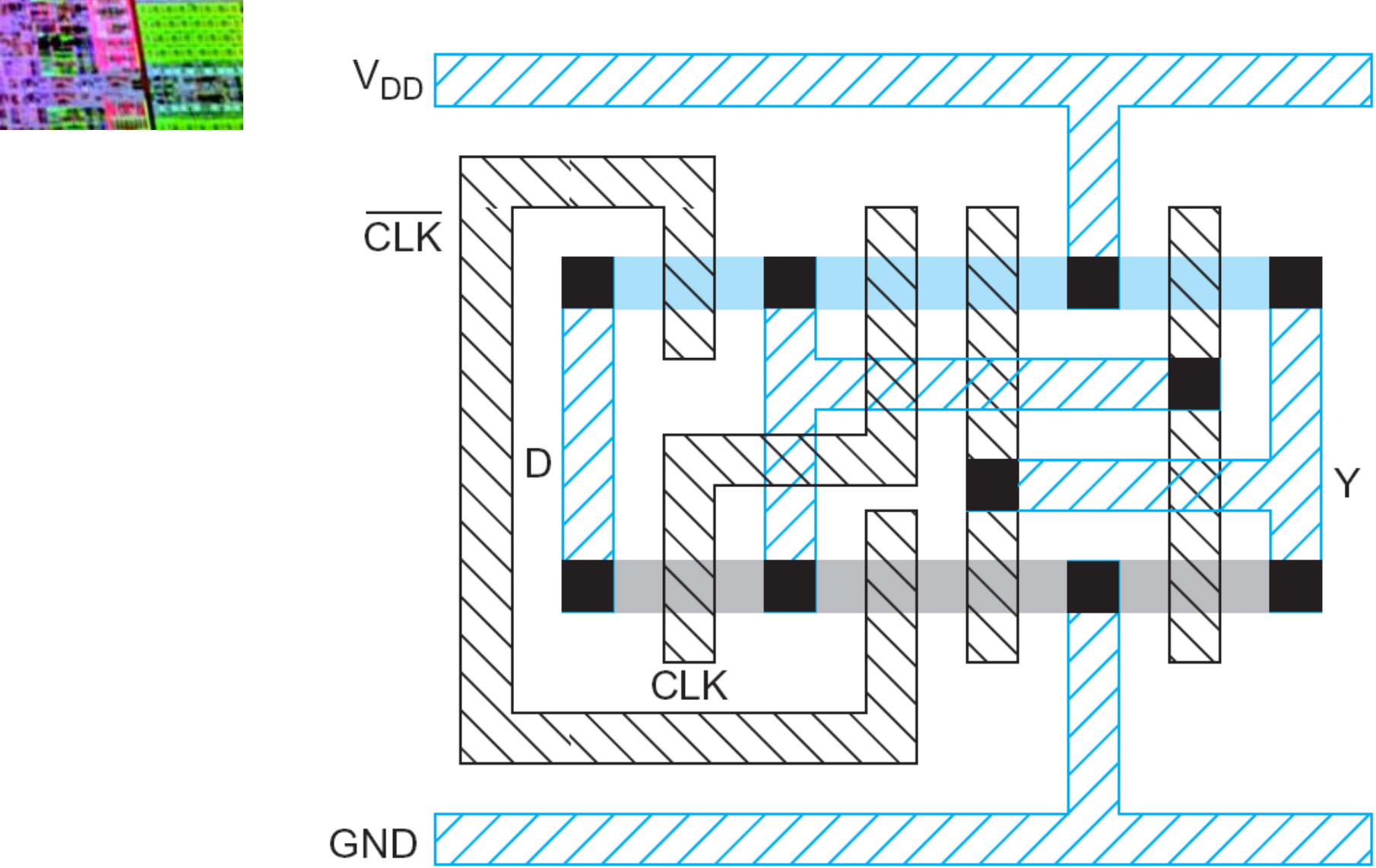

FIGURE 1.75 Level-sensitive latch stick diagram

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